Call For Papers

2nd IEEE International Workshop on Defect and Fault Tolerant Nanoscale Architectures (NANOARCH'06)

To be held in conjunction with the International Symposium on Computer Architecture

June 17, 2006

Boston Park Plaza Hotel, Boston, MA, USA

Current defect tolerance, fault-tolerance and manufacturing test techniques are designed under the assumption that a system under test is composed largely of correctly functioning units. However, this assumption is severely tested in emerging nanoelectronics such as molecular electronics, quantum electronics, single electron transistors and carbon nanotubes and nanowires. In these nanoelectronics, self-assembly based fabrication results in failures rates an order of magnitude higher than in traditional CMOS. Consequently, defect and fault tolerance -at the physical, circuit and most importantly at the system level- is an enabling technology for building reliable nanoelectronic systems.

NANOARCH will investigate novel defect and fault tolerance architectures targeting these highly unreliable nanoelectronics. The workshop will be a forum for presenting theoretical, simulation and case studies on new defect models, defect and fault tolerance architectures, associated experimental reliability evaluation and validation frameworks and computer aided simulation and design tools for these emerging nanoelectronics. Topics of interest include but are not limited to:

- Defect tolerant nanoelectronic architectures at device, circuit, and system level
- Fault tolerant nanoelectronic architectures at the device, circuit, and system level
- Emerging computational paradigms for nanoelectronics
- Modeling and simulation of novel nanoelectronic architectures and concepts
- Implementing micro-architectural concepts using nanoarchitectural building blocks
- Dynamic reconfiguration in nanoelectronic architectures
- Defect and fault models in emerging nanoelectronic device technologies
- Manufacture testing methodologies for nanoelectronic architectures
- Yield models, yield analysis and yield enhancement in nanoelectronics
- CAD targeting defect and fault-tolerant nanoelectronic architectures

The Program Committee invites authors to submit papers up to 8 pages in length, describing original, unpublished recent work. Clearly describe the nature of the work, explain its significance, highlight novel features, and describe its current status. Electronic submission through the workshop website is required.

The submission of a paper proposal will be considered evidence that upon acceptance, the author(s) will present their paper at the workshop. Final versions of accepted papers will be included in the NANOARCH *Workshop Digest.*

Important deadlines:

Abstracts: March 20, 2006 **Paper: March 27, 2006**

Acceptance notification: May 1, 2006 **Final version of papers: June 1, 2006**

For up-to-date workshop information: www.nanoarch.org