Call for Papers:
IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH'09)
Co-located with IEEE/ACM Design Automation Conference, San Francisco, CA, USA
www.nanoarch.org

Important Dates
Paper submission: May 28, 2009
Acceptance notification: June 21, 2009
Final version: July 7, 2009
Symposium: July 30-31, 2009

Moore's law based scaling is rapidly approaching a "brick wall" as we enter the nanoelectronic regime. Novel silicon and non-silicon nanoelectronic devices are being developed to explicitly address this problem. Similarly, while defect and fault-tolerance techniques are designed under the assumption that a system is composed largely of correctly functioning units, this is no longer true in emerging nanoelectronics. In addition, nanoelectronics offers massive parallelism on a scale significantly beyond anything we have seen before, yet very few commercial massively parallel applications are envisioned. Also, while current computer aided design tools and methodologies can barely manage billion-transistor chips, how can trillion-device chips that nanoelectronics promises be designed?

The purpose of the NANOARCH symposium is to be a forum for the presentation and discussion of novel architectures and design methodologies by considering these issues in future nanoscale implementations. The symposium seeks to build on the successes of the first four iterations of NANOARCH (2005-2008). NANOARCH is interested in novel architectures including massively parallel, biologically inspired as well as those that are defect and fault tolerant, case studies on defect, fault and yield models, experimental reliability evaluation, validation frameworks, computer aided simulation, and design tools and emerging computational models for nanoelectronics. The symposium's topics of interest include:

* Architectures for nanoelectronic digital and mixed-signal circuits and systems
* Computational paradigms and programming models for nanoscale architectures
* Modeling and simulation of nanoelectronic devices, circuits and system architecture
* Simulation of complex systems with nanoscale computing architectures
* Implementing microarchitecture concepts using nanoarchitecture building blocks
* Defect and fault tolerant nanoelectronic device, circuit, and system level architectures
* Manufacture testing of nanoelectronic architectures
* Computer aided design tools and methodologies for nanoelectronic architectures

The Program Committee invites authors to submit extended abstracts (2 pgs) or full papers (up to 6 pgs) describing original, unpublished recent work. Clearly describe the nature of the work, explain its significance, highlight novel features, and describe its current status. Electronic submission through the symposium website is required. The submission of an abstract or paper proposal will be considered evidence that upon acceptance, the author(s) will present this work at the symposium. The final versions of accepted abstracts/papers will be included in the NANOARCH Symposium Proceedings. Full papers will be considered for the inaugural NANOARCH Best Paper recognition.

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