18.12.2023
-
20.12.2023

18TH INTERNATIONAL SYMPOSIUM ON NANOSCALE ARCHITECTURES IN DRESDEN, GERMANY

PROGRAM BOOKLET

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CONFERENCE AT A GLANCE

	Monday (18.12.)
08:30	Registration & Welcome Address
09:00	Keynote 1: Subhasish Mitra
10:15	Coffee Break
10:30	
11:00	Regular Session 1
12:00	
12:30	Lunch
13:00	
13:30	Invited Talk 1: Hussam Amrouch
14:00	
14:15	Coffee break
14:45	
15:00	Industry Session Panelist Talks
16:00	
16:15	Coffee break
16:30	Industry Session
17:00	Panel Discussion
17:30	Welcome Reception and Guided City Tour
18:00	see page 22
evening	

Tuesday (19.12.)	Wednesday (20.12.)
Registration	Registration
Keynote 2: Tony Kenyon	Tutorial Session: Fernando Corinto & Georgios Ch. Sirakoulis
Coffee Break	Coffee Break
Invited Talk 2: Karl Leo	
	Regular Session 5
Regular Session 2	
	Lunch
Lunch	
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Regular Session 3	Coffee break
Coffee break	
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Coffee break	
Invited Talk 3: Gianaurelio Cuniberti	Regular Session 7
Gala Dinner see page 24	Farewell & Best Paper Award Ceremony

GENERAL CHAIR'S MESSAGE

Prof. Dr. Ronald Tetzlaff

General Chair

Welcome to Dresden!

As we gather in the vibrant city of Dresden, the heart of Europe's microelectronics innovation, it is my great pleasure to extend a warm welcome on behalf of the Organizing Committee and of the Steering Committee to all participants of the 18th ACM International Symposium on Nanoscale Architectures (NANOARCH). This symposium has been a flagship of nanotechnology and advanced computing research since its inception in 2005, continuously unfolding novel dimensions in the field. This NANOARCH version is sponsored by the Association for Computing Machinery (ACM), the German Research Foundation (DFG) and by TUD | Dresden University of Technology.

This year's NANOARCH will be a rich ground for breakthrough ideas and pioneering research. Our symposium will cover a broad spectrum of topics ranging from unconventional transistor technologies and advanced neural network architectures to the intricacies of quantum computation and the evolving landscape of spin-based electronics. We will journey through the frontiers of energy-efficient logic systems, dimensional computing paradigms, and the adaptive learning dynamics in advanced memristor systems. This wide-ranging and profound exploration of topics signifies our unwavering commitment to fostering

innovation and achieving excellence in the ever-evolving fields of nanotechnology and computing. In addition, I am more than proud to welcome a number of outstanding invited speakers who are coming to Dresden to share their knowledge with the NANOARCH audience.

All these talks and discussions are set against the backdrop of Dresden – rightfully dubbed as the Microelectronics Center of Europe – a city where history, culture, and technological innovation converge in a spectacular fashion. Dresden is proud for its dense concentration of semiconductor industries and synergistic academia-industry collaborations in microelectronics, supported by strategic geographical advantages and robust governmental support. This vibrant ecosystem not only reflects the city's rich technological heritage but also positions it at the forefront of global innovation and research in the microelectronics sector.

I would like to extend my heartfelt gratitude to all the members of the organizing and scientific boards, our funding organizations, our dedicated volunteers, and the vibrant community of researchers, without whom this conference would not have been possible. Your commitment, expertise, and passion are the pillars that uphold the spirit and success of NANOARCH. As we embark on this exciting journey over the next three days, I encourage you to engage, collaborate, and be inspired. Dresden offers a unique blend of historical richness and modern innovation – the perfect setting for fostering creative ideas and lasting connections.

Here's to a conference filled with enlightening discussions, groundbreaking insights, and, most importantly, joy and fun in the realm of nanotechnology and computing!

Welcome to ACM NANOARCH 2023 – where the future of nanotechnology is not just discussed but shaped.

Ronald Tetzlaff

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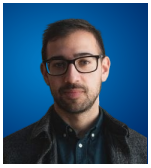

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GENERAL INFORMATION

CONFERENCE VENUE

NANOARCH 2023 will be held in the **Dülfer Hall**, located in the Alte Mensa (old university canteen) of TU Dresden, which claims to be the oldest university dining hall of Germany. The Dülfer Hall, a multipurpose event room of TU Dresden's Rectorate, is named after the renowned architect Martin Dülfer, known for his contributions to architecture in the late 19th and early 20th centuries. Dülfer was a pioneer of the Jugendstil movement in Germany, which is the German equivalent of Art Nouveau, and his architectural style is noted for its innovative and decorative elements.

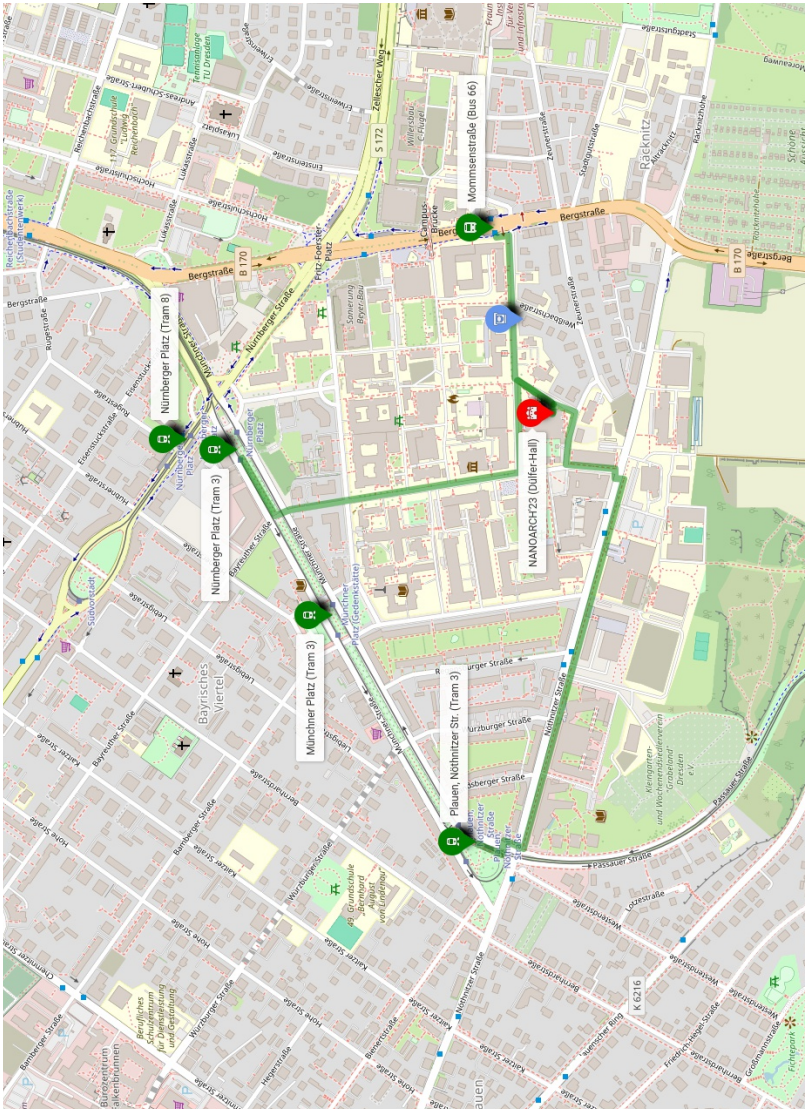
Address

Dülfersaal, Building M13 Mensa, TU Dresden, Floor (Etage) 01
Mommsenstraße 13
01069 Dresden

- Distance to main main station (by foot): 1.6 km
- Distance to Dresden airport (by car): 14 km
- Distance to the "Frauenkirche" (by foot): 3.4 km
- Distance to the "Zwinger/Alte Meister" (by foot): 3.4 km

CONFERENCE MAP

Online: https://t1p.de/NANOARCH2023-map



GENERAL INFORMATION

CONFERENCE REGISTRATION DESK

The Conference Registration Desk is located inside Dülfer Hall:

Monday, December 18:	07:30 - 19:00
Tuesday, December 19:	08:00 - 17:15
Wednesday, December 20:	08:00 - 18:00

ON-SITE REGISTRATION

On-site registration for the conference will be conducted during the registration desk hours by the registration chair.

DRESDEN

Dresden's beauty is inseparable from the natural beauty of the Elbe valley. City and landscape have developed harmoniously over centuries. Its architectural character has been shaped by masterpieces from numerous eras. The best-known historical attractions of the old city include the Zwinger, the Cathedral, the Semper Opera House, the Royal Palace, and the Frauenkirche, which was reconstructed with donations from all over the world. The Neustadt district is furthermore the largest wholly preserved late-19th-century city quarter in Germany.
Actually, Dresden has over 563.000 inhabitants and is one of the biggest cities of Saxony. Dresden welcomes you also with some chocolate, a pencil and a note block in your bag and we hope that you will enjoy your stay here in our beautiful city of Dresden.

For further information about Dresden please follow the link below:
https://www.dresden.de/index_en.php

CURRENCY EXCHANGE AND CREDIT CARDS

Only Euros are accepted in stores and restaurants. You can obtain Euros at ATM, at foreign exchange banks and other authorized money exchanges. Banks are closed on Saturdays and Sundays. Most German services accept major credit cards. However, smaller shops tend to prefer cash.

☐☐☐☐ ELECTRICITY & INTERNET / WIFI

The electricity supply in Germany is 230 V, 50 Hz.

Since NANOARCH 2023 will be held within the facilities of TU Dresden, we expect most of the participants to have a strong WiFi connection via **eduroam**. If you do not have such access, please let us know so we can prepare special guest credentials for you.

☐☐☐☐ INSURANCE

The conference organizers cannot accept liability for personal injuries sustained, for loss of or damage to property belonging to conference participants (or their accompanying persons), either during or as a result of the conference. Please check the validity of your own insurance.

☐☐☐☐ OFFICIAL LANGUAGE

English will be used for all presentations and printed matter. No interpretation service will be provided.

☐☐☐☐ TIME DIFFERENCE

The time in Germany during winter is Central European Time (CET = UTC+1).

☐☐☐☐ LUNCHES, DINNER AND COFFEE BREAKS

Lunches, coffee breaks, welcome reception and gala dinner are included in the registration fee.

☐☐☐☐ HELPFUL PHONE NUMBERS

Police	110
Emergency rescue / fire fighters	112
Taxi	+49 351 211 211

CONFERENCE BAG

GIFT BAG

The bag was specially designed for the conference. The skyline of Dresden is placed above the logo. In addition to the conference slogan, logos of the main organizing and supporting organizers are shown. The bag contains an USB flash drive with conference information as well as Dresden and Christmas typical gifts and sweets.

"RÄUCHERHÄUSCHEN" - SMOKER HOUSES

Smoker houses are a popular type of incense burner that are often used as part of traditional Christmas decorations. The house is in two parts and the upper part can be removed from the base plate. This base plate shows a spot, where the incense candles are placed and lit. A lighter or match can be used for this. The tip of the incense candle should glow (no flame). The house is then placed back on the base plate. The smoke will now be released through the chimney in proper style, spreading a wonderful Christmas scent.

STOLLEN KONFEKT

Stollen is a sweet bread traditionally baked at Christmas. It contains nuts, spices, and dried or candied fruit, coated with powdered sugar or icing sugar and often containing marzipan. Slices are usually cut and eaten in the same way as savoury bread. However, there are also so-called Stollen confectionery - handy, bite-sized pieces of the popular Christmas bread.

USB FLASH DRIVE

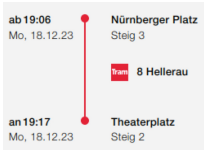
The USB flash drive, that you have found in your NANOARCH gift bag, is special. On the one hand, it contains this program booklet and the conference proceedings, which is common. On the other hand, it contains a Live-USB operating system that we call “Uni flash drive” - another unique aspect of TU Dresden. The flash drive is based on Linux Debian and contains lots of free and open source software (FOSS) that is valueable for students and scientists. Try it by booting from the stick!

WELCOME RECEPTION EVENING

AGENDA

Monday, 18.12.2023

17:30 - 18.50	Dinner at Dülfer Saal: Flying Buffet & Drinks with Band "Sammelsurium"
18:50 - 19.05	Walk from Dülfersaal to tram station "Nürnberger Platz" next to drugstore "dm"
19.06 - 19.17	Tram Ride to "Theaterplatz" Tram Nr. 8, direction "Hellerau"
19.30 - 20.30	Guided City Tour with Stollen Baker Grete
20.30 - open	Free evening on Christmas market / in city center



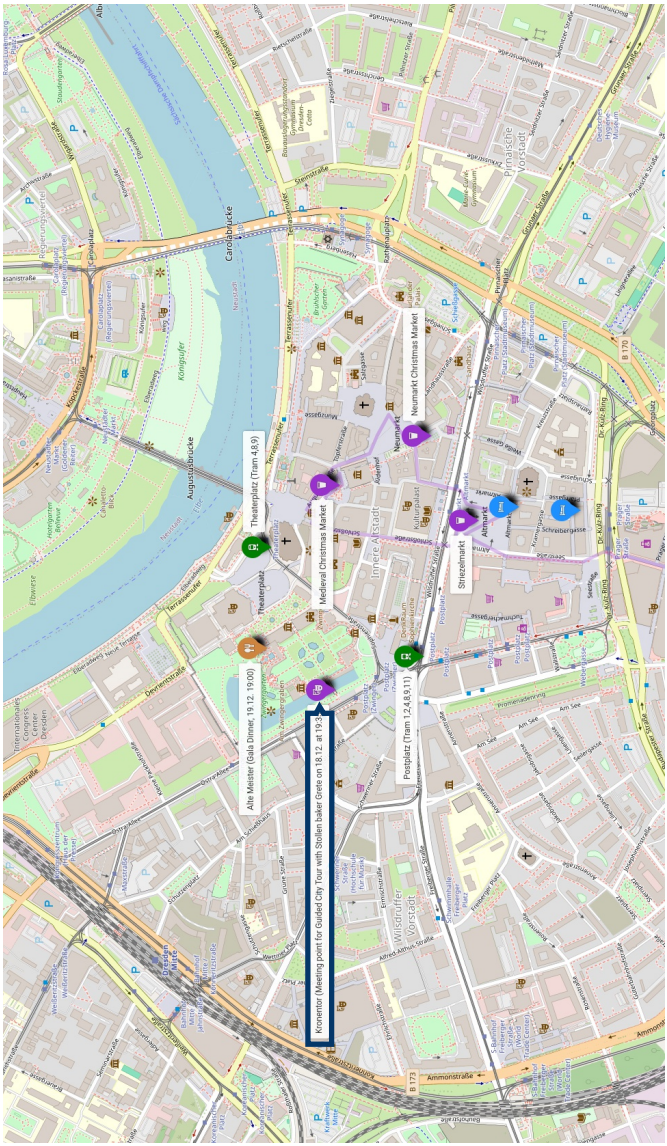
STOLLEN BAKER GRETE

Dessert after dinner will be served on the city tour with Stollen Baker "Grete". On a culinary city tour through Christmassy Dresden, Grete will talk about typical Saxon delicacies and Dresden's inventive baking culture. She will also talk about the history of the "Striezel" and the city's past with its most important buildings. The tour will be accompanied by sweets and a hot drink.

TRADITIONAL CHRISTMAS MARKET "STRIEZELMARKT"

Dresden's Striezelmarkt is not only the oldest Christmas market in Germany, it is also one of the most famous in the world. It offers more than 200 beautifully adorned market huts where you can find delicious treats and wonderful gift ideas. The entertainment programme includes dancing, singing, a vibrant itinerary for children, as well as concerts and traditional festivities.

MAP - TRAM STATION AND MEETING POINT CITY TOUR



GALA DINNER EVENING

AGENDA
Tuesday, 19.12.2023

- 19:00 Start Dinner at Alte Meister Restaurant
  Common first and second course
  Choice for main course (asked during beginning of dinner)
  Drinking flatrate for cremant/wine/beer/soft drinks/coffee
- 21:30 Desertbuffet in the associated historic French pavilion
  Live music by the band "Stilbruch"

RESTAURANT "ALTE MEISTER"

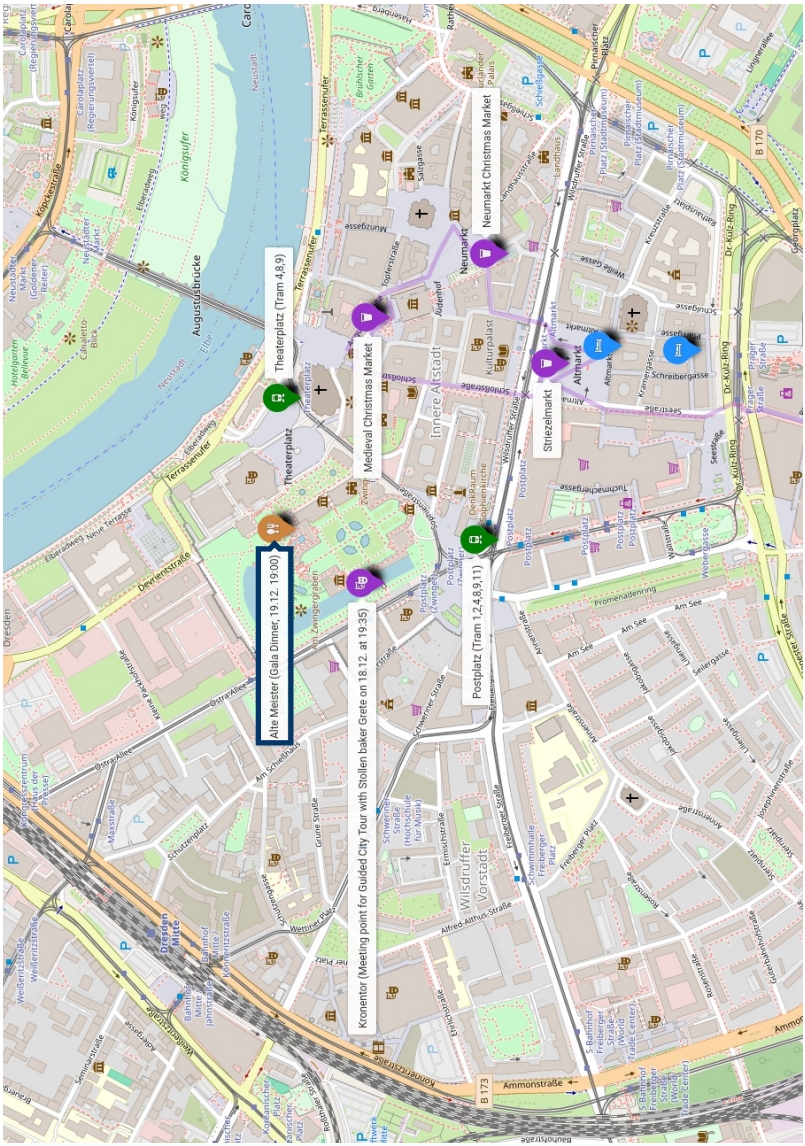
Address
Theaterplatz 1A
01067 Dresden

The "Alte Meister" Restaurant is the perfect place to meet in the historic heart of Dresden, whether for lunch, coffee or dinner. It is located next to the "Alte Meister Galerie" - a famous painting gallery with outstanding works by German, French, and Spanish painters from the 15th to the 18th centuries.

LIVE BAND "STILBRUCH"

With violin, cello, drums and vocals, three classically trained musicians with many years of experience have been delighting their fans throughout Europe with their self-composed German and English songs since 2005. Cellist Sebastian Maul and violinist Antonio Palanovic develop a mesmerising stage presence by playing their instruments standing up and singing at the same time. Konstantin Chiddi on drums provides the driving beats which, together with the two string instruments, make up Stilbruch's unique crossover sound.

MAP - TRAM STATION AND MEETING POINT CITY TOUR



INVITED SPEAKER

KEYNOTE 1

Time: Monday, 09:00 - 10:15

"The Future of Hardware Technologies for Computing"

Subhasish Mitra
William E. Ayer Professor
Dept. of Electrical Engineering & Dept. of Computer Science
Stanford University

Chair: Ronald Tetzlaff

Abstract

The computation demands of 21st-century abundant-data workloads, such as AI/machine learning, far exceed the capabilities of today's computing systems. For example, a Dream AI Chip would ideally co-locate all memory and compute on a single chip, quickly accessible at low energy. Such Dream Chips aren't realizable today. Computing systems instead use large off-chip memory and spend enormous time and energy shuttling data back and forth. This memory wall gets worse with growing problem sizes, especially as conventional transistor miniaturization gets increasingly difficult.

The next leap in computing requires transformative NanoSystems by exploiting the unique characteristics of nanotechnologies and abundant-data workloads. We create new chip architectures through ultra-dense 3D integration of logic and memory – the N3XT 3D approach. Multiple N3XT 3D chips are integrated through a continuum of chip stacking/interposer/wafer-level integration — the N3XT 3D MOSAIC. To scale with growing problem sizes, new Illusion systems orchestrate workload execution on N3XT 3D MOSAIC creating an illusion of a Dream Chip with near-Dream energy and throughput.

Several hardware prototypes, built in commercial and research fabrication facilities, demonstrate the effectiveness of our approach. We target 1,000X system-level energy-delay-product benefits, especially for abundant-data workloads. We also address new ways of ensuring robust system operation despite growing challenges of design bugs, manufacturing defects, reliability failures, and security attacks.

Short Bio

Subhasish Mitra is William E. Ayer Professor in the Departments of Electrical Engineering and Computer Science at Stanford University. He is also the Associate Chair (Faculty Affairs) of Computer Science. Prof. Mitra directs the Stanford Robust Systems Group, leads the Computation Focus Area of the Stanford SystemX Alliance, and is a member of the Wu Tsai Neurosciences Institute. His research ranges across Robust Computing, NanoSystems, Electronic Design Automation (EDA), and Neurosciences. Results from his research group have influenced almost every contemporary electronic system, and have inspired significant government and research initiatives in multiple countries. He has held several international academic appointments — the Carnot Chair of Excellence in NanoSystems at CEA-LETI in France, Invited Professor at EPFL in Switzerland, and Visiting Professor at the University of Tokyo in Japan. Prof. Mitra also has consulted for major technology companies including Cisco, Google, Intel, Samsung, and Xilinx (now AMD).

In the field of Robust Computing, he has created many key approaches for circuit failure prediction, on-line diagnostics, QED system validation, soft error resilience, and X-Compact test compression. Their adoption by industry is growing rapidly, in markets ranging from cloud computing to automotive systems. His X-Compact approach has proven essential for cost-effective manufacturing and high-quality testing of almost all 21st century systems, enabling billions of dollars in cost savings.

With his students and collaborators, he demonstrated the first carbon nanotube computer. They also demonstrated the first 3D NanoSystem with computation immersed in data storage. These received wide recognition: cover of NATURE, Research Highlight to the US Congress by the NSF, and highlight as "important scientific breakthrough" by global news organizations.

Prof. Mitra's honors include the Harry H. Goode Memorial Award (by the IEEE Computer Society for outstanding contributions in the information processing field), Newton Technical Impact Award in EDA (test-of-time honor by ACM SIGDA and IEEE CEDA), the University Researcher Award (by the Semiconductor Industry Association and Semiconductor Research Corporation to recognize lifetime research contributions), the Intel Achievement Award (Intel's highest honor), and the US Presidential Early Career Award. He and his students have published over 10 award-winning papers across 5 topic areas (technology, circuits, EDA, test, verification) at major venues including the Design Automation Conference, International Solid-State Circuits Conference, International Test Conference, Symposium on VLSI Technology, Symposium on VLSI Circuits, and Formal Methods in Computer-Aided Design. He is an ACM Fellow, an IEEE Fellow, and a Distinguished Alumnus of the Indian Institute of Technology, Kharagpur.

INVITED SPEAKER

INVITED TALK 1

Time: Monday, 13:30 - 14:15

"In-Memory Computing using Ferroelectric Transistors: Lessons Learnt and Future Trends"

Hussam Amrouch
Professor of AI Processor Design
School of Computation, Information and Technology
Technical University of Munich

Chair: Fernando Corinto

Abstract
In the burgeoning realm of artificial intelligence (AI), the pursuit of In-Memory Computing (IMC) is paramount. This relentless pursuit, aimed at catalyzing ultra-fast and energy-efficient AI computations, is emblematic of the cutting-edge innovations at the nexus of Ferroelectric FET (FeFET) technology. In this talk, we will showcase the latest advancements in FeFETs, spanning from traditional IMC-based hardware accelerators to monolithic 3D integration using advanced back-end-of-line (BEOL) thin-film transistors. We will elucidate the inherent challenges posed by ferroelectric stochasticity along with temperature effects, and demonstrate innovative strategies, such as using thermoelectric devices for advanced on-chip cooling, to mitigate their adverse impacts, paving the way for reliable computing using FeFET-based IMC.

Short Bio
Hussam Amrouch is a W3-Professor heading the Chair of AI Processor Design at the Technical University of Munich. He is, additionally, heading the Brain-inspired Computing at the Munich Institute of Robotics and Machine Intelligence (MIRMI). Further, he is the head of the Semiconductor Test and Reliability at the University of Stuttgart. He received his Ph.D. degree with the highest distinction (summa cum laude) from KIT in 2015. He has around 220 publications (including more than 90 journals) in multidisciplinary research areas starting from device physics to circuit design and HW/SW co-design. His research interest is brain-inspired computing using emerging technologies with a special focus on reliability. He has served in the technical program committees in all major EDA conferences and as a reviewer in many top journals like Nature Electronics, Nature Communications. He is also as Editor at the Nature Scientific Reports journal.

KEYNOTE 2

Time: Tuesday, 09:00 - 10:15

"Engineering memristors for memory, neuromorphic computing and beyond"

Anthony Kenyon
Professor of Nanoelectronic & Nanophotonic Materials
Dept. of Electronic & Electrical Eng.
University College London

Chair: Neil Kemp

Abstract
Computing hardware is at a critical stage in its evolution. Our current AI computing demands, driven largely by the development of advanced Artificial Neural Networks (ANNs) whose compute demands currently double every 2-3 months, are rapidly becoming unsustainable. New approaches are needed, and memristive devices and systems are a set of technologies that offer significant promise. In this talk I will review the prospects for memristors to make a decisive contribution to the future of computing. I will address challenges around materials engineering, device design, and the adoption of new technologies by the CMOS industry.

Short Bio
Anthony (Tony) Kenyon is Professor of Nanophotonic and Nanoelectronic Materials at University College London (UCL), where he also serves as Vice Dean (Strategy) for the Faculty of Engineering Sciences. His research interests cover memristive materials and devices, silicon photonics, nanophotonics and nanoelectronics. He has worked for more than a decade on silicon oxide (SiOx) memristive devices, probing the physics of resistance switching and demonstrating new modes of operation. Along with Dr Adnan Mehonic he co-founded Intrinsic Semiconductor Technologies Ltd to commercialise SiOx RRAM for non-volatile memories. Tony is a Fellow of the IoP and the IET, a Senior Member of the IEEE and is currently the President of the European Materials Research Society.

INVITED SPEAKER

INVITED TALK 2

Time: Tuesday, 10:30 - 11:15

"Organic semiconductors: from displays to neuromorphic"

Karl Leo
Chair of Opto-Electronics
Dresden Integrated Center for Applied Physics and Photonic Materials (IAPP), Technische Universität Dresden

Chair: Ronald Tetzlaff

Abstract
Organic semiconductors are based on carbon compounds and allow an almost inexhaustible variety of materials. Devices based on organic semiconductors enable a variety of novel applications for flexible, lightweight, and environmentally friendly electronics. A first application success are OLED displays, which have already conquered a double-digit billion market and dominate the market in mobile phones. In this talk, I introduce the material class of organic semiconductors and show with some examples from doping to organic solar cells the challenges of materials research and the implementation in products. Furthermore, vertical organic transistors with greatly improved properties are discussed, including bipolar transistors which open the GHz range for organic electronics. Finally, an outlook is given on a new form of neural networks based on organic semiconductors, allowing highly efficient neuromorphic computing approaches.

Short Bio

Prof. Karl Leo studied physics in Freiburg I. Br. and Stuttgart and was postdoc at AT & T Bell Laboratories and the RWTH Aachen. In 1993, he became professor of optoelectronics at the TU Dresden. He is the head of the Institute of Applied Physics and director of the interdisciplinary center "Dresden Integrated Center for Applied Physics and Photonic Materials (DC IAPP)", which bundles the research to organic semiconductors at the TU Dresden.

Prof. Karl Leo is an internationally recognized researcher in condensed matter physics. Among his achievements are the first observations of coherent electronic dynamics in solids (quantum beats and Bloch oscillations in semiconductor superlattices) and pioneering work on organic semiconductors, including the successful introduction of controlling doping in organic components; electronic components with world record efficiency (OLED, organic solar cells) and maximum frequency (organic transistors), and the first realisation of organic inversion transistors. Many of these technologies were successfully transferred to spin-off companies like Novaled and Heliatek. His main current research interests are novel organic electronic devices (Organic Devices and Structures group) and organic sensors (Organic Sensors group).

Prof. Leo has been rewarded with the Leibniz Award 2002 of the DFG, the German Future Award 2011 of the German President and the European Inventors Award 2021 of the European Patent Office.

INVITED SPEAKER

INVITED TALK 3

Time: Tuesday, 16:45 - 17:30

"Digital olfaction"

Gianaurelio Cuniberti
Institute for Materials Science and Max Bergmann Center for Biomaterials
Dresden Center for Computational Materials Science (DCMS)
Technische Universität Dresden

Chair: Neil Kemp

Abstract
Olfaction, an ancient sensory system, provides intricate information about the environment. In emulation of this biological process, neuromorphic devices in conjunction with machine learning algorithms, endeavor to replicate and digitize the olfactory capabilities. This presentation focuses on the gas discrimination and identification capabilities of neuromorphic nanosensors. These nanosensors, constructed with functionalized nano materials, were integrated into multi-channel gas sensor devices, and their sensing signals were recorded upon exposure to diverse gases. The temporal characteristics of the gases were subsequently extracted from the sensing signals and input into a machine learning algorithm to discern and identify the specific gases. The resulting electronic olfaction system demonstrates outstanding gas identification performance across various gases. This innovative platform has the potential to downsize electronic noses, digitize olfactory information, and distinguish a range of gases and volatile organic compounds (VOCs). Applications include pathogen detection, environmental monitoring, and disease diagnosis.

Short Bio

Professor Gianaurelio Cuniberti holds since 2007 the Chair of Materials Science and Nanotechnology at the Technische Universität Dresden (TU Dresden) and the Max Bergmann Center of Biomaterials in Dresden, Germany. He is a member of the TU Dresden School of Engineering Sciences (Materials Science) and of the School of Science (Physics). He studied Physics at the University of Genoa, Italy (where he got his B.Sc. and M.Sc.) and obtained his Ph.D. in 1997 at the age of 27 in a joint collaboration between the University of Genoa and the University of Hamburg, Germany. He was visiting scientist at MIT and the Max Planck Institute for the Physics of Complex Systems Dresden. From 2003 to 2007, he was the head of a Volkswagen Foundation Research Group at the University of Regensburg, Germany. His research activity is internationally recognized in more than 400 scientific journal papers to date. He initiated and organized numerous workshops, schools, and conferences and took part in international research training networks, offering extensive opportunities for young scientists. He has given plenary and invited talks at numerous international meetings. He serves as a referee for numerous high-impact journals and for several funding research institutions including among others the EU, the German Science Foundation (DFG), the USA National Science Foundation (NSF), the German Israeli Foundation (GIF), and the Alexander von Humboldt Foundation.

He received several talent scholarships and awards including the Max Planck Society Schloeßmann Award (2001) and the VolkswagenStiftung Research Group Individual Grant (2003). He is a member of several scientific organizations and a corresponding member of the Umbrian Academy of Sciences. Gianaurelio Cuniberti is an Honorary Professor at the Division of IT Convergence Engineering of POSTECH, the Pohang University of Science and Technology since 2009, since 2011 Adjunct Professor for the Department of Chemistry at the University of Alabama, and since 2019 Guest Professor at SJTU. In 2018 he became a faculty member of the transcampus between TU Dresden and King's College London.

Professor Gianaurelio Cuniberti is an elected member of the European Academy of Sciences, of the Academia Europaea and of the Germany National Academy of Science and Engineering (acatech).

INVITED SPEAKER

TUTORIAL SESSION:
OSCILLATION-BASED COMPUTING WITH MEMRISTORS

Time: Wednesday, 09:00 - 09:45

"Memristor-based Oscillatory Platforms for Pattern Recognition: from nano-device to bioinspired algorithms"

Fernando Corinto
Full Professor - Politecnico di Torino, Italy

Chair: Alon Ascoli

Abstract
One of the most fascinating areas of research is the strive for designing a neuromorphic or brain simulating system, where specialized algorithms run on a brain-inspired microprocessor may replicate the dynamical behavior of the vast network of synapse-coupled neurons. Current digital supercomputers are able to reproduce some of the brain functionalities, but, as more and more intelligent operations are emulated, the consequent increases in power consumption and integrated circuit area are somewhat unacceptable. These increases are due to the inefficient classical Von- Neumann architecture, which is at the basis of the machine design and is characterized by a rigid adherence to Boolean logic and, above all, by the separation between the physical location where data are stored, i.e. the memory, and the physical location where data processing takes place, i.e. the Computing Power Unit. In addition to that, complex integration of information performed by biological neural systems is based on several dynamical mechanisms. Among them, the most worth is the synchronization of neural activity. Synchronization of neural activity is also one of the proposed solutions to a widely discussed question in neuroscience: the binding problem, i.e. how our brain bind all the different data together to recognize objects. Despite remarkable progress has been made in the field of Neurophysiology and Nonlinear Dynamics needed to understand neural structures and interactions, current brain-simulating systems require high-computational capabilities to reproduce only a few brain functionalities.

The tutorial aims to present the fundamental theory of memristor oscillatory networks, their nonlinear dynamical properties, including synchronization, bifurcation phenomena and spatio-temporal pattern formation, for information processing tasks.

References

[1] D. E. Nikonov et al., “Coupled-oscillator associative memory array operation for pattern recognition,” IEEE J. Explor. Solid-State Comput. Devices Circuits, vol. 1, pp. 85–93, 2015.

[2] A. Ascoli, S. Slesazeck, H. Mähne, R. Tetzlaff, and T. Mikolajick, “Nonlinear dynamics of a locally- active memristor,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 4, pp. 1165–1174, Apr. 2015.

[3] S. Kumar, J. P. Strachan, and R. S. Williams, “Chaotic dynamics in nanoscale NbO2 Mott memristors for analogue computing,” Nature, vol. 548, no. 7667, pp. 318–321, Aug. 2017.

[4] M. Escudero et al., "Chua’s Circuit With Tunable Nonlinearity Based on a Nonvolatile Memristor: Design and Realization," in IEEE Transactions on Circuits and Systems I: Regular Papers, doi: 10.1109/TCSI.2023.3323854.

[5] M. Escudero et al., “Physical implementation of a tunable memristorbased Chua’s circuit,” in Proc. IEEE 48th Eur. Solid State Circuits Conf. (ESSCIRC), Sep. 2022, pp. 117–120.

[6] M. D. Marco, M. Forti, L. Pancioni, G. Innocenti, A. Tesi, and F. Corinto, “Oscillatory circuits with a real non-volatile Stanford memristor model,” IEEE Access, vol. 10, pp. 13650–13662, 2022.

[7] F. Corinto, M. Forti, and L. O. Chua. "Nonlinear Circuits and Systems with Memristors." Nonlinear Dynamics and Analogue Computing via the Flux-Charge Analysis Method. Springer Verlag. Available online at: https://www. springer. com/gp/book/9783030556501 (2020).

This activity is part of the project Analoge COmputing with Dynamic Switching Memristor Oscillators: Theory, Devices and Applications (COSMO), Grant PRIN 2017LSCR4K 002, funded by the Italian Ministry of Education, University and Research (MIUR).

INVITED SPEAKER

Short Bio

Fernando Corinto received the Master's Degree in Electronic Engineering and the Ph.D. degree in Electronics and Communications Engineering from the Politecnico di Torino, in 2001 and 2005 respectively. He also received the European Doctorate from the Politecnico di Torino, in 2005. Prof. Corinto was awarded a Marie Curie Fellowship in 2004.

He is currently Full Professor of Electrical Engineering with the Department of Electronics and Telecommunications, Politecnico di Torino.

His research activities are mainly on nonlinear dynamical circuits and systems, complex/neural nonlinear networks and memristor technology for machine learning and optimization problems.

Prof. Corinto is co-author of 4 books, 10 book chapters and more than 170 international journal and conference papers. Since 2010, he is Senior Member of the IEEE. He is also Member of the IEEE CAS Technical Committees on "Cellular Nanoscale Networks and Array Computing" and "Nonlinear Circuits and Systems". Prof. Corinto served as Vice-Chair of the IEEE North Italy CAS Chapter. Prof. Corinto has been Associated Editor of the IEEE Trans. on Circuits and Systems - I for 2014-2015. He is also in the Editorial Board and Review Editor of the International Journal of Circuit Theory and Applications since January 2015. Prof. Corinto has been the Vice Chair of the COST Action "Memristors - Devices, Models, Circuits, Systems and Applications (MemoCiS)". Prof. Corinto has been DRESDEN Senior Fellows at the Technische Universität Dresden in 2013 and 2017. Prof. Corinto is also August-Wilhelm Scheer visiting professor at Technische Universität München and member of the Institute for Advanced Study - Technische Universität München.

TUTORIAL SESSION

Time: Wednesday, 09:45 - 10:15

"Wave memristive oscillatory circuits: A multifunctional computing perspective"

Georgios Ch. Sirakoulis
Full Professor - Democritus University of Thrace, Greece

Chair: Alon Ascoli

Short Bio

Georgios Ch. Sirakoulis received his Diploma degree in Electrical and Computer Engineering (1996) from the Democritus University of Thrace (DUTh), Greece, and for his Diploma Thesis he received a prize of distinction from the Technical Chamber of Greece (TEE). In 2001, he received his PhD in Electrical and Computer Engineering from the Democritus University of Thrace, Greece. He is a Professor and the Head of the Department of Electrical and Computer Engineering, DUTh. He has published more than 340 technical papers. He is the Co-editor of seven books, the Co-author of 32 book chapters, and the Guest Editor of 16 special issues.

His research interests include future and emergent electronic devices, circuits, models, and architectures, unconventional computing, memristors, cellular automata, quantum cellular automata, bioinspired computation/biocomputation and bioengineering, and modeling and simulation. He is the Editor of IEEE TRANSACTIONS ON NANOTECHNOLOGY, IEEE Nanotechnology Magazine, Microelectronics Journal, Integration, VLSI Journal, and the Journal of Cellular Automata. He is in TCs of IEEE CASS, like TC Cellular Nanoelectronics and Gigascale Systems (Nano-Giga) (as Chair), TC IEEE Cellular Nanoscale Networks and Array Computing Technical Committee (CNN-MAC) (as Secretary), IEEE Nanotechnology Council, VP-Publications Chair of IEEE NTC (2024-present), NTC Technical Committee on Nanoelectronics, Vice Chair of IEEE Task Force on Unconventional Computing, and IEEE Greece Section Treasurer.

INVITED SPEAKER

INVITED TALK 4

Time: Tuesday, 13:30 - 14:15

"Memristive and CMOS Technologies for Advanced Cognitive Systems"

Erika Covi
Senior Scientist — Cognitive Systems, NaMLab gGmbH;
Incoming Assistant Professor - Zernike Institute for Advanced Materials (ZIAM) & Groningen Cognitive Systems and Materials Center (CogniGron) - University of Groningen
Chair: Fernando Corinto

Abstract
In the past two decades, the shift towards a distributed computing paradigm led our smart systems to become more and more interconnected. These systems need to elaborate increasingly amount of data while featuring low-power operation, area efficiency, and ability to interact with the external world in real time. Memristive technology, with its unique characteristics and capabilities, holds great promise for the design of such cognitive systems. The potential for energy-efficient and parallel computing, combined with the ability to integrate complex neural and synaptic dynamics within a single device, provides avenues for high-performance hardware implementations. Moreover, by offering volatile and non-volatile memory in a small footprint, enabling dense integration, and facilitating in-memory computing, memristive technology presents advantages that, if correctly combined with CMOS technology, can extend the functionality of current artificial intelligent systems.
In this talk, we discuss the challenges and the opportunities to realise memristive neuromorphic computing by developing novel hardware architectures and learning algorithms specifically tailored to best exploit the intrinsic properties of memristive technology. Indeed, we show that memristive technology offers vast potential, but its effective utilization relies on the synergetic development of memristive devices, circuits, and algorithms to create performing hardware cognitive systems.

Short Bio

Dr. Erika Covi is currently Senior Scientist at NaMLab gGmbH, Dresden (Germany), where she is the leader of the Cognitive Systems group. Starting from 1st January 2024, she will join the Zernike Institute for Advanced Materials & Groningen Cognitive Systems and Materials Center (Groningen, the Netherlands) as assistant professor. She received her PhD in Microelectronics in 2014 from the University of Pavia (Italy), where she worked on designing integrated systems for the characterisation of memristive devices. Before joining NaMLab, she worked at the National Research Council (CNR) of Italy first, then at Politecnico di Milano (Italy).

She was awarded with an ERC Starting Grant for the project MEMRINESS on the development of memristive neurons and synapses for neuromorphic edge computing in 2021.

Her research interests lie at the intersection of emerging devices, circuit design, and brain-inspired computing. More specifically, they focus on exploiting the intrinsic physical characteristics of memristive devices to reproduce computational primitives of the brain in mixed neuromorphic-memristive systems.

INDUSTRY PANEL

PANELISTS (ALPHABETICAL ORDER)

Dr. Sven Beyer

Distinguished Member of Technical Staff - Integration (eNVM)
GlobalFoundries

Dr. Albrecht Kieslich

Head of Process Integration
Robert Bosch Semiconductor Manufacturing Dresden GmbH

Mr. Matthias Lohrmann

Co-founder & Chief Technology Officer (CTO)
SpiNNcloud Systems GmbH

Prof. Thomas Mikolajick

Scientific Director
NaMLab gGmbH
Chair of Nanoelectronics, TU Dresden

AGENDA

- 14:45-16:15 Panelist Talks
- 16:15-16:30 Coffee Break
- 16:30-17:30 Panel Discussion

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REGULAR SESSION 1: ADVANCED COMPUTING ARCHITECTURES AND SYSTEMS

CHAIR : IOANNIS MESSARIS

A Spatial-Designed Computing-In-Memory Architecture Based on Monolithic 3D Integration for High-Performance Systems

Time: Monday, 10:30 - 10:48

Keywords: Monolithic 3D, Computing-in-memory, Neural network accelerator, Hardware architecture, DNN mapping algorithm

Jiaming Li (School of Integrated Circuits, Beijing Innovation Center for Future Chips, BNRist, Tsinghua University, Beijing, China), Bin Gao (School of Integrated Circuits, Beijing Innovation Center for Future Chips, BNRist, Tsinghua University, Beijing, China), Ruihua Yu (School of Integrated Circuits, Beijing Innovation Center for Future Chips, BNRist, Tsinghua University, Beijing, China), Peng Yao (School of Integrated Circuits, Beijing Innovation Center for Future Chips, BNRist, Tsinghua University, Beijing, China), Jianshi Tang (School of Integrated Circuits, Beijing Innovation Center for Future Chips, BNRist, Tsinghua University, Beijing, China), He Qian (School of Integrated Circuits, Beijing Innovation Center for Future Chips, BNRist, Tsinghua University, Beijing, China) and Huaqiang Wu (School of Integrated Circuits, Beijing Innovation Center for Future Chips, BNRist, Tsinghua University, Beijing, China).

Abstract

The computing-in-memory (CIM) technology effectively addresses the bottleneck of data movement in traditional von-Neumann architecture, especially for deep neural network (DNN) acceleration. However, with the improving performance and parallelism of CIM processing elements (PEs), the substantial latency and power overhead caused by high-density intermediate results transmission has become a new bottleneck in CIM architectures. In this paper, we propose a spatial-designed CIM architecture based on the emerging Monolithic 3D (M3D) technology, and a spatiality-aware DNN mapping method for high-performance CIM systems. The proposed architecture introduces a novel hierarchy by implementing staggered tiers, enabling PEs to be shared by multiple tiles, and uses the ultra-dense and lower-power Inter-

Layer Vias (ILVs) in M3D as shared buses, enabling CIM PEs to exploit the ultra-high bandwidth of M3D for inter-tile and intra-tile data transfer. Our experiment result shows that the proposed M3D-enabled CIM architecture, combined with the proposed mapping method, achieves a 6.52x latency improvement, a 40.84x interconnection energy-delay product (EDP) improvement, and a 7.62x system-level EDP improvement compared to state-of-the-art CIM architecture.

Minimal Design of SiDB Gates: An Optimal Basis for Circuits Based on Silicon Dangling Bonds

Time: Monday, 10:48 - 11:06

Keywords: Emerging Technology, Post-CMOS, Gate Design

Jan Drewniok (Technical University of Munich), Marcel Walter (Technical University of Munich) and Robert Wille (Technical University of Munich/Software Competence Center Hagenberg GmbH).

Abstract

Silicon Dangling Bonds (SiDBs) present a promising computational technology that goes beyond traditional CMOS. It enables the creation of circuitry using single atoms as elementary components. Since current computational technologies approach their physical limits, SiDBs have attracted significant interest from both academia and industry. More precisely, single SiDBs allow for realizing Boolean functionality. They form gates which, then, are utilized as fundamental building blocks to realize arbitrary circuit logic. However, although, fabrication capabilities are advancing rapidly and initial design automation methodologies have been proposed, the current design of these gates is primarily based on manual methods. This paper presents an approach

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capable of designing SiDB gates using the minimum number of SiDBs possible for a given Boolean function, and thus, minimizing gate cost. In addition to the guaranteed minimality, this allows to design SiDB gates, which require significantly fewer SiDBs compared to gate designs currently used in the state of the art. This breakthrough simplifies SiDB circuit designs and their corresponding manufacturing processes significantly, thereby accelerating the progress of this promising technology.

Post-Layout Optimization for Field-Coupled Nanotechnologies

Time: Monday, 11:06 - 11:24

Keywords: Field-coupled Nanocomputing, Physical Design, Placement and Routing, Post-Processing,

Simon Hofmann (Technical University of Munich), Marcel Walter (Technical University of Munich) and Robert Wille (Technical University of Munich & SCCH GmbH).

Abstract

While conventional computing technologies reach their limits, the demand for computation power keeps growing, fueling the interest in post-CMOS technologies. One promising contestant in this domain is Field-coupled Nanocomputing (FCN), which conducts computations based on the repulsion of physical fields at the nanoscale. However, to realize a dedicated functionality in this technology design methods are needed that create corresponding FCN layouts. While several methods for FCN layout generation have been proposed in the past, the underlying complexity requires them to resort to heuristic approaches—leading to results of sub-par quality and offering room for improvement. In conventional CMOS design, post-layout optimization methods are available to exploit this potential for further improvement.

Unfortunately, no such methods exists yet for FCN. In this work, we are addressing this gap and introduce the first post-layout optimization approach for FCN. Experimental evaluations show the benefits of the approach: Applied to layouts generated by two complementary state-of-the-art methods, the proposed post-layout optimization allows for a further area reduction of 50.79 % and 20.00 % on average, respectively—confirming the potential of post-layout optimization for FCN.

Memristor-based Network Switching Architecture for Energy Efficient Cognitive Computational Models

Time: Monday, 11:24 - 11:42

Keywords: Memristors, Switches, Energy Efficiency

Saad Saleh (University of Groningen) and Boris Koldehofe (TU Ilmenau).

Abstract

The Internet makes use of high performance network switches in-order to route network traffic from end users to servers. Despite line-rate performance, the current switches consume huge energy and lack the ability to support more expressive learning models, like neuromorphic functions. The major reason is the use of transistors in the underlying Ternary Content Addressable Memory (TCAM) which is volatile and supports digital computations only. These shortcomings can be bypassed by developing network memories building on novel components, like Memristors, due to their nonvolatile, nanoscale and analog storage/processing characteristics. In this paper, we propose the use of a novel memristor-based pCAMCogniGron memory which provides both digital (deterministic) and analog (probabilistic) outputs for supporting cognitive computational models in network switches. The traditional digital

REGULAR SESSION 1: ADVANCED COMPUTING ARCHITECTURES AND SYSTEMS

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operations can still be supported by a memristor-based energy efficient TCAM, called TCAmMCogniGron. Building on pCAMCogniGron and TCAmMCogniGron, we propose a novel network switching architecture and analyze its energy efficiency over the experimental dataset of a Nb-doped SrTiO3 memristive device. The results show that the proposed network switching architecture consumes only 0.01 fJ/bit/cell energy for analog compute operations which is 50 times less than the transistor-based TCAM.

LUT-based RRAM Model for Neural Accelerator Circuit Simulation

Time: Monday, 11:42 - 12:00

Keywords: Neural Accelerator, Memristor, RRAM, Artificial Neural Network, Lookup Table

Max Uhlmann (IHP – Leibniz Institut fuer innovative Mikroelektronik), Tommaso Rizzi (IHP – Leibniz Institut fuer innovative Mikroelektronik), Jianan Wen (IHP – Leibniz Institut fuer innovative Mikroelektronik), Emilio Pérez-Bosch Quesada (IHP – Leibniz Institut fuer innovative Mikroelektronik), Bakr Al Beattie (Ruhr University Bochum), Karlheinz Ochs (Ruhr University Bochum), Eduardo Pérez (IHP – Leibniz Institut fuer innovative Mikroelektronik), Philip Ostrovskyy (IHP – Leibniz Institut fuer innovative Mikroelektronik), Corrado Carta (IHP – Leibniz Institut fuer innovative Mikroelektronik), Christian Wenger (IHP – Leibniz Institut fuer innovative Mikroelektronik) and Gerhard Kahmen (IHP – Leibniz Institut fuer innovative Mikroelektronik).

Abstract

Neural hardware accelerators have been proven to be energy-efficient when used to solve tasks which can be mapped into an artificial neural network (ANN) structure. Resistive random-access memories (RRAMs) are currently under investigation together with several different memristive devices as promising technologies to build such accelerators combined together with complementary metal-oxide semiconductor (CMOS)-technologies in integrated circuits (ICs).

While many research groups are actively developing sophisticated physical-based representations to better understand the underlying phenomena characterizing these devices, not much work has been dedicated to exploit the trade-off between simulation time and accuracy in the definition of low computational demanding models suitable to be used at many abstraction layers. Indeed, the design of complex mixed-signal systems as a neural hardware accelerators requires frequent interaction between the application- and the circuit-level that can be enabled only with the support of accurate and fast-simulating devices' models.

In this work, we propose a solution to fill the aforementioned gap with a lookup table (LUT)-based Verilog-A model of IHP's 1-transistor-1-RRAM (1T1R) cell. In addition, the implementation challenges of conveying the communication between the abstract ANN simulation and the circuital analysis are tackled with a design flow for resistive neural hardware accelerators that features a custom Python wrapper. As a demonstration of the proposed design flow and 1T1R model, an ANN for the MNIST handwritten digit recognition task is assessed with the last layer verified in circuit simulation. The obtained recognition confidence intervals show a considerable discrepancy between the purely application-level PyTorch simulation and the proposed design flow which spans across the abstraction layers down to the circuital analysis.

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CHAIR : IOANNIS MESSARIS

Resilience and Precision Assessment of Natural Language Processing Algorithms in Analog In-Memory Computing: A Hardware-Aware Study

Time: Monday, 12:30 - 12:18

Keywords: AIMC, NLP, DNN, PCM

Amirhossein Parvaresh (Ilmenau University of Technology), Shima Hosseinzadeh (Friedrich-Alexander University Erlangen-Nürnberg) and Dietmar Fey (University Erlangen-Nuremberg).

Abstract

Natural Language Processing (NLP) serves as a cornerstone technology, facilitating complex human-computer interactions, enabling information retrieval, conducting sentiment analysis, and enhancing language comprehension. With the ever-growing use of NLPs, the conventional 'von Neumann' computing paradigm is rapidly approaching its inherent limitations. In response, Analog In-Memory Computing (AIMC) emerges as a compelling alternative, albeit accompanied by inherent non-idealities when deploying neural networks on such platforms. In this paper, we have evaluated the precision and resilience of various NLP algorithms when executed within the AIMC framework, both with and without the application of hardware-aware training. Our analysis reveals noteworthy insights: Gated Recurrent Unit (GRU) neural networks exhibit enhanced resilience to noise, yielding an average test error of 3.97% following hardware-aware training, as compared to their full precision counterparts. Conversely, Long Short-Term Memory (LSTM) networks demonstrate a slightly higher average test error of 5.67%, indicating a relatively lower tolerance to non-idealities. In contrast, Convolutional Neural Networks (CNNs) manifest a heightened vulnerability, exhibiting an average relative test error of 13.34%.Furthermore, we systematically investigate the sensitivity profiles of the selected neural networks in the presence of specific non-idealities, providing valuable insights into their robustness and susceptibility within the AIMC environment.

VLCP: A High-Performance FPGA-based CNN Accelerator with Vector-level Cluster Pruning

Time: Monday, 12:18 - 12:36

Keywords: Convolutional Neural Network (CNN), Hardware Accelerator, Model Compression

Shuo Ran (Nanjing University of Aeronautics and Astronautics (NUAA)), Bi Wu (Nanjing University of Aeronautics and Astronautics (NUAA)), Ke Chen (Nanjing University of Aeronautics and Astronautics (NUAA)) and Weiqiang Liu (Nanjing University of Aeronautics and Astronautics (NUAA)).

Abstract

Convolutional neural networks (CNNs) are widely used in computer vision, natural language processing, and other application scenarios. But deploying CNNs at the edge is challenging due to their large number of parameters. Pruning is a solution that can effectively reduce the number of parameters and off-chip memory accesses. However, high sparsity unstructured pruning is not hardware-friendly, while structured pruning has low compression efficiency. As a result, vector-level pruning, with a coarser granularity, is a promising alternative that balances pruning performance and hardware-friendliness. In this paper, a hardware-oriented vector-level pruning strategy is proposed based on the CNN vector distribution properties. By expanding the dynamic range of vector groups, more important weights can be preserved without sacrificing accuracy. When applied to the VGG-16 and ResNet-18 models on the ImageNet dataset, the proposed strategy achieved 10.93X and 10.17X compression ratios in convolutional layers with a 66% reduction in computation and an acceptable drop in top-1 accuracy. Furthermore, the proposed pruning scheme achieves a remarkable performance of 188 FPS on the VCU118 evaluation board, demonstrating its compatibility with hardware. Compared to the state-of-the-art, the proposed strategy reaches 69% performance improvement and up to 2.8X higher LUT efficiency.

REGULAR SESSION 2: NEUROMORPHIC COMPUTING AND NEURAL NETWORKS

CHAIR : FARHAD MERCHANT

Towards Temporal Information Processing – Printed Neuromorphic Circuits with Learnable Filters

Time: Tuesday, 11:15 - 11:33

Keywords: printed electronics, neuromorphic computing, temporal information processing, recurrent neural network

Haibin Zhao (Karlsruhe Insitute of Technology), Priyanjana Pal (Karlsruhe Insitute of Technology), Michael Hefenbrock (RevoAI GmbH), Michael Beigl (Karlsruhe Insitute of Technology) and Mehdi B. Tahoori (Karlsruhe Insitute of Technology).

Abstract

With the progression of Internet of Things, many novel consumer products such as wearable devices and disposable electronics requires flexibility, biocompatibility and ultra low-costs. However, these features can hardly be matched by traditional silicon-based electronics. In this regard, printed electronics becomes one of the most competitive candidate by offering the aforementioned properties thanks to its additive manufacturing process. To address fundamental signal-processing tasks, printed neuromorphic circuits, emulating the artificial neural networks, have received increasing attention, as they can achieve appealing computational capabilities by assembling simple elemental circuit primitives. However, many target applications for printed electronics are based on processing temporal sensory data, which is beyond the reach of existing printed neuromorphic circuits, since they lack components with time dependencies. To this end, this paper proposes a novel printed temporal processing block that combines existing circuit primitives with a sequence of learnable low-pass filters. We model the proposed circuit and proposed the corresponding training objective to enable the bespoke design of the circuits. Simulations on 15 benchmark time-series datasets reveal that, in comparison to existing printed neuromorphic circuits, the proposed circuits can effectively process temporal

information by using 1.5× and 1.3× of device counts and power respectively. Moreover, the achieved classification accuracy reaches 98% of that from classic hardware-agnostic Elman recurrent neural networks.

Material and Physical Reservoir Computing for Beyond CMOS Electronics: Quo Vadis?

Time: Tuesday, 11:33 - 11:51

Keywords: reservoir computing, material computing, neural network, neuromorphic, hardware, beyond CMOS

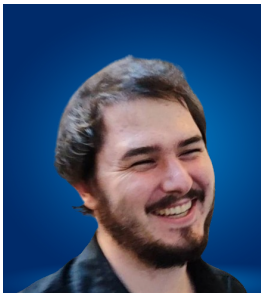
Christof Teuscher (Portland State University).

Abstract

Traditional computing is based on an engineering approach that imposes logical states and a computational model upon a physical substrate. Physical or material computing, on the other hand, harnesses and exploits the inherent, naturally-occurring properties of a physical substrate to perform a computation. To do so, reservoir computing is often used as a computing paradigm. In this review and position paper, we take stock of where the field currently stands, delineate opportunities and challenges for future research, and outline steps on how to get material reservoir to the next level. The findings are relevant for beyond CMOS and beyond von Neumann architectures, ML, AI, neuromorphic systems, and computing with novel devices and circuits.

REGULAR SESSION 2: NEUROMORPHIC COMPUTING AND NEURAL NETWORKS

CHAIR : FARHAD MERCHANT



Non Volatile Operators Emulation Platform

Time: Tuesday, 11:51 - 12:09

Keywords: FPGA, RISC-V, FeFET, Emulation, Logic in Memory

Alban Nicolas (Institut des Nanotechnologies de Lyon), Cédric Marchand (Institut des Nanotechnologies de Lyon) and David Navarro (Institut des Nanotechnologies de Lyon).
Non Volatile Operators Emulation Platform.

Abstract

The Von-Neumann bottleneck is one of the biggest problem to achieve higher computing performances and energy efficiency, especially in data centric applications. One of these application, the Internet of Things (IoT), is expanding at an impressive pace and is relying massively on sensors with limited energy to work. The emergence of new CMOS compatible technologies like ferroelectric field effect transistor (FeFET) allows to design new kind of Logic-in-Memory (LiM) operators. These non-volatile operators are expected to help overcoming the Von-Neumann Bottleneck as it will retain information thanks to the non volatility of the FeFET. The amount of data transfer will decrease thanks to this particularity. However, design of new computing operators is a long process. It is important to know if these operators are interesting to pursue into further development, which is why they need to be evaluated. To this extent, we present in this article a Non-volatile Operators Emulation Platform. the platform is based on the COMET RISC-V processor and use emulation to evaluate the impact of new non-volatile memories based operator on the processor performances in terms of number of instruction.

Neural Network Modeling Bias for Hafnia-based FeFETs

Time: Tuesday, 12:09 - 12:27

Keywords: ferroelectric field effect transistor (FeFET) emerging device modeling, hardware neural network, neuromorphic hardware

Osama Yousuf (George Washington University), Imtiaz Hossen (George Washington University), Andreu Glasmann (DEVCOM Army Research Laboratory), Sina Najmaei (DEVCOM Army Research Laboratory) and Gina Adam (George Washington University).

Abstract

As the landscape of integrated electronics confronts fundamental limitations of conventional Complementary Metal-Oxide Semiconductor (CMOS) technology, the need for investigating novel post-CMOS device technologies in the context of deep learning has significantly grown, both in simulation and in prototyping. In this work, modeling bias – the difference between the test accuracy obtained by a reference network prototype and a simulated model of that prototype – is explored in the context of hafnia-based ferroelectric field effect transistor (FeFET) devices. Device operating conditions are investigated as a parameter for mitigating the impact of device-to-device variability on the underlying network performance. The computational framework includes a physics-based compact model with artificial variance to sample device data and a multivariate Kriging model to create jump table device models; this framework is a fast and efficient technique to model device populations for realistic neural network simulations. The performance of a 2-layer perceptron network – where each synapse is realized via an FeFET device in a crossbar-based training scheme – is investigated on the Modified National Institute of Standards and Technology (MNIST) dataset for classification. Results suggest that devices with low variability and high dynamic range generally attain good network performance, and that the device gate read voltage Vgs can be optimized to tradeoff between the two. This study elucidates novel insights regarding the capability of Hafnia-based FeFET devices as bit-limited synapses for classification problems, and thus, serves as an important guideline for future investigations into experimental prototypes of FeFET-based networks and other types of neuromorphic circuits.

REGULAR SESSION 2: NEUROMORPHIC COMPUTING AND NEURAL NETWORKS

CHAIR : FARHAD MERCHANT

Multiplexer Optimization for Adders in Stochastic Computing

Time: Tuesday, 12:27 - 12:45

Keywords: Adder optimization, Multiplexers, Neural networks, Stochastic computing

Sercan Aygun (University of Louisiana at Lafayette), M. Hassan Najafi (University of Louisiana at Lafayette), Lida Kouhalvandi (Dogus University) and Ece Olcay Gunes (Istanbul Technical University).

Abstract

This study presents an optimization algorithm for multiplexer (MUX)-based scaled adders. In stochastic computing (SC), simple multiplication and accumulation operations are performed using an XNOR gate and MUX. Scaled adders represent cascaded 2^m-to-1 MUXs and facilitate the accumulation of multiple terms. The optimization of these adders assumes significance in cases involving accumulation of a large number of terms. The depth of cascaded MUXs varies with m, which in turn, affects their area, delay, and accuracy. The proposed algorithm performs stage-wise optimization of m. As observed, the proposed approach increases the noisy-dataset classification accuracy of SC-based neural networks by 3.61%.

REGULAR SESSION 3:
HARDWARE AND SYSTEM OPTIMIZATIONS

CHAIR : ASAL KIAZADEH

Reducing the Complexity of Operational Domain Computation in Silicon Dangling Bond Logic

Time: Tuesday, 13:45 - 14:03

Keywords: Silicon Dangling Bonds, Field-coupled Nanocomputing, Operational Domain, Simulation

Marcel Walter (Technical University of Munich), Jan Drewniok (Technical University of Munich), Samuel Sze Hang Ng (University of British Columbia), Konrad Walus (University of British Columbia) and Robert Wille (Technical University of Munich & SCCH GmbH).

Abstract

Silicon Dangling Bonds (SiDBs) constitute a beyond-CMOS computational nanotechnology platform that enables higher integration density and lower power consumption than contemporary CMOS nodes. Recent manufacturing breakthroughs in the domain sparked the interest of academia and industry alike in the race for a green computation future at the nanoscale. However, as the fabrication of SiDBs requires atomic precision, SiDB logic systems are inherently susceptible to environmental defects and material variations, which inevitably occur. The Operational Domain is a methodology to evaluate the resilience of SiDB logic against physical parameter variations. However, state-of-the-art implementations require a quadratic number of exponentially complex physical simulator calls to assess the operational domain. This paper presents two novel algorithms to obtain operational domains in an efficient fashion: one based on flood fill, and one based on contour tracing. Experimental evaluations confirm that they reduce the number of required simulator calls by 70.87% and 95.29%, respectively. Particularly contour tracing achieves the shift from a quadratic to a linear relation, thereby reducing the complexity and paving the way for realizing reliable SiDB-based computing systems.

REGULAR SESSION 3: HARDWARE AND SYSTEM OPTIMIZATIONS

CHAIR : ASAL KIAZADEH

Accurate and Energy-Efficient Stochastic Computing with Van Der Corput Sequences

Time: Tuesday, 14:03 - 14:21

Keywords: Deterministic sequences, Emerging computing, Image processing, Pseudo-random sources, Quasi-random number generators, Stochastic computing

Mehran Shoushtari Moghadam (University of Louisiana at Lafayette), Sercan Aygun (University of Louisiana at Lafayette), Mohsen Riahi Alam (University of Louisiana at Lafayette), Jonas I Schmidt (University of Louisiana at Lafayette), M. Hassan Najafi (University of Louisiana at Lafayette) and Nima Taherinejad (Heidelberg University).

Abstract

In stochastic computing (SC), data is represented using random bitstreams. The efficiency and accuracy of SC systems rely heavily on the stochastic number generator (SNG), which converts data from binary to stochastic bit-streams. While previous research has shown the benefits of using low-discrepancy (LD) sequences like Sobol and Halton in the SNG, the potential of other well-known random sequences remains unexplored. This study investigates new random sequences for potential use in SC. We find that Van Der Corput (VDC) sequences hold promise as a random number generator for accurate and energy-efficient SC, exhibiting intriguing correlation properties. Our evaluation of VDC-based bit-streams includes basic SC operations (multiplication and addition) and image processing tasks like image scaling. Our experimental results demonstrate high accuracy, reduced hardware cost, and lower energy consumption compared to state-of-the-art methods.

Heterogeneous Instruction Set Architecture for RRAM-enabled In-memory Computing

Time: Tuesday, 14:21 - 14:39

Keywords: heterogeneous computing, instruction set architecture, RRAM, in-memory computing, machine learning

Houji Zhou (School of Integrated Circuits, Huazhong University of Science and Technology), Zhiwei Zhou (School of Integrated Circuits, Huazhong University of Science and Technology), Shengguang Ren (School of Integrated Circuits, Huazhong University of Science and Technology), Jia Chen (AI Chip Center for Emerging Smart Systems, InnoHK, HongKong, China), Yi Li (School of Integrated Circuits, Huazhong University of Science and Technology, Hubei Yangtze Memory Laboratories) and Xiangshui Miao (School of Integrated Circuits, Huazhong University of Science and Technology, Hubei Yangtze Memory Laboratories).

Abstract

RRAM-enabled in-memory computing (IMC) is regarded as a promising solution for breaking the von Neumann bottleneck. Using RRAM-based IMC to construct heterogeneous computing systems can fully leverage the advantages of both digital and IMC platforms. Critical challenges are effectively managing the dataflows between the digital system and the analog IMC and providing a standard for communication. In this paper, from the perspective of hardware instruction execution, we designed a general RRAM-enabled analog instruction set architecture compatible with digital computing. These instructions adopted the vector-based computing concepts in RISC-V, and the examples compatible with RISC-V vector extension are demonstrated in detail. A tile-processing unit-array three-level architecture is also devolved to support the instruction execution. The hardware estimations are performed on 65 nm technology. Results indicate that the total activated power of the activated processing unit is 8.64 mW which is 4.9 times smaller than PUMA and 33.4 times smaller than ISAAC. The energy efficiency reaches 1190.7 GOPS/W, 1.42x and 3.12x compared with PUMA and ISAAC, respectively. Furthermore, as the analog and digital computing frequency increases, the peak energy efficiency can reach 40 TOPS/W which enables the future general use of the IMC-based heterogeneous system.

REGULAR SESSION 3: HARDWARE AND SYSTEM OPTIMIZATIONS

CHAIR : ASAL KIAZADEH

A Robust Time-based Error-Proofing Readout Scheme for MRAM

Time: Tuesday, 14:39 - 14:57

Keywords: MRAM, time-based readout scheme, phase detector, improved BER

Qianlei Ou (School of Integrated Circuit Science and Engineering, Beihang University), Shixing Li (School of Integrated Circuit Science and Engineering, Beihang University), Chao Wang (School of Electronics and Information Engineering, Beihang University), He Zhang (School of Computer Science and Engineering, Beihang University) and Zhaohao Wang (School of Integrated Circuit Science and Engineering, Beihang University).

Abstract

A time-based readout scheme with adjustable time resolution for magnetic random access memory (MRAM) is proposed. An improved error-proofing circuit utilizing phase detector (PD) is also designed to reduce bit error rate (BER). The strong robustness of the proposed circuits is verified using Monte Carlo simulations.

REGULAR SESSION 4:
NOVEL TECHNOLOGIES AND FUTURE NETWORKS

CHAIR : GINA ADAM

Hyper Dimensional Computing with Ferroelectric Tunneling Junctions

Time: Tuesday, 15:15 - 15:33

Keywords: Hyper Dimensional Computing, HDC, Ferroelectric Tunneling Junction, FTJ

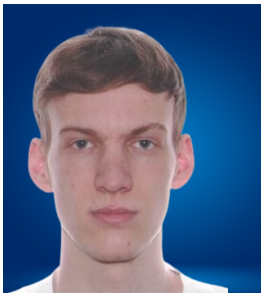
Stefan Slesazeck (NaMLab), Suzanne Lancaster (NaMLab), John Reuben (Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU)), Shima Hosseinzadeh (Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU)), Dietmar Fey (Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU)) and Thomas Mikolajick (NaMLab / TU Dresden).

Abstract

Hyper Dimensional Computing is a new approach in artificial intelligence (AI). The specific requirements of massive parallel readout operation during HDC inference makes the high-impedance ferroelectric tunneling junction (FTJ) devices a very interesting candidate for the hardware realization of a HDC accelerator. Therefore, we propose to research both, the technological and the architectural constraints when bringing together this two distinct concepts from the architectural and the devices perspective.

REGULAR SESSION 4: NOVEL TECHNOLOGIES AND FUTURE NETWORKS

CHAIR : GINA ADAM



Spin Wave Threshold Logic Gates

Time: Tuesday, 15:33 - 15:51

Keywords: Spintronics, Spin Waves, Threshold Logic

Arne Van Zegbroeck (TU Delft), Pantazis Anagnostou (TU Delft), Said Hamdioui (TU Delft), Christoph Adelmann (IMEC), Florin Ciubotaru (IMEC) and Sorin Cotofana (TU Delft).

Abstract

While Spin Waves (SW) interaction provides natural support for low power Majority (MAJ) gate implementations many hurdles still exists on the road towards the realization of practically relevant SW circuits. In this paper we leave the SW interaction avenue and propose Threshold Logic (TL) inspired SW computing, which relies on successive phase rotations applied to one single SW instead of on the interference of an odd number of SWs. After providing a short TL inside we introduce the SW TL gate concept and discuss the way to mirror TL gate weight and threshold values into physical phase shifter's parameters. Subsequently, we design and demonstrate proper operation of a SW TL based Full Adder (FA) by means of micro-magnetic simulations. We conclude the paper by providing inside on the potential advantages of our proposal by means of a conceptual comparison of MAJ and TL based FA implementations.

Exploring Multi-Valued Logic and its Application in Emerging Post-CMOS Technologies

Time: Tuesday, 15:51 - 16:09

Keywords: Multi-valued logic computing, post-CMOS technologies, Resistive RAM, ISFET

Simranjeet Singh (Indian Institute of Technology Bombay, Forschungszentrum Juelich), Elmira Moussavi (RWTH Aachen University), Christopher Bengel (RWTH Aachen University), Sachin Patkar (Indian Institute of Technology Bombay), Rainer Waser (RWTH Aachen University, Forschungszentrum Juelich), Rainer Leupers (RWTH Aachen University), Vikas Rana (Forschungszentrum Juelich), Vivek Pachauri (RWTH Aachen University), Stephan Menzel (Forschungszentrum Juelich) and Farhad Merchant (Newcastle University).

Abstract

Multi-valued logic (MVL), characterized by more than two possible logic states, presents distinct advantages compared to conventional Boolean logic. Novel post-CMOS technologies, particularly memristive and bio-sensitive devices, exhibit compelling attributes that make them promising candidates for realizing MVL computing components. To assess the viability of these devices, we delve into key aspects of Memristive and ISFETs, including their state transition dynamics, multi-level functionality, and compatibility with CMOS manufacturing processes. Through this investigation, we successfully demonstrate the practical implementation of ternary arithmetic MVL gates utilizing memristive and bio-sensitive devices. Our findings affirm that these innovative devices hold the potential to serve as MVL computing elements effectively.

REGULAR SESSION 4: NOVEL TECHNOLOGIES AND FUTURE NETWORKS

CHAIR : GINA ADAM

Concept paper on novel radio frequency resistive switches

Time: Tuesday, 16:09 - 16:27

Keywords: Wireless communication, memristors, 6G network

Asal Kiazadeh (i3N/CENIMAT, NOVA School of Science and Technology, Campus de Caparica), Jonas Deuermeier (i3N/CENIMAT, NOVA School of Science and Technology, Campus de Caparica), Emanuel Carlos (i3N/CENIMAT, NOVA School of Science and Technology, Campus de Caparica), Rodrigo Martins (i3N/CENIMAT, NOVA School of Science and Technology, Campus de Caparica), Sergio Matos (Instituto Universitário de Lisboa and Instituto de Telecomunicacoes), Fabio Martinho Cardoso (Instituto Universitário de Lisboa and Instituto de Telecomunicacoes), Luis Manuel Pessoa (INESC TEC and Faculty of Engineering, University of Porto)

Abstract

For reconfigurable radios where the signals can be easily routed from one band to another band, new radiofrequency switches (RF) are a fundament. The main factor driving the power consumption of the reconfigurable intelligent surface (RIS) is the need for an intermediate device with static power consumption to maintain a certain surface configuration state. Since power usage scales quadratically with the RIS area, there is a relevant interest in mitigating this drawback so that this technology can be applied to everyday objects without needing such a high intrinsic power consumption. Current switch technologies such as PIN diodes, and field effect transistors (FETs) are volatile electronic devices, resulting in high static power. In addition, dynamic power dissipation related to switching event is also considerable. Regarding energy efficiency, non-volatile radio fre-quency resistive switch (RFRS) concept may be better alternative solution due to several advantages: smaller area, zero-hold voltage, lower actuation bias for operation, short switching time, scalability and capable to be fabricated in the backend-of-line of standard CMOS process.

REGULAR SESSION 5:
MEMRISTOR AND RRAM TECHNOLOGIES

CHAIR : CHRISTOF TEUSCHER

A Behavioural Compact Model for Programmable Neuromorphic ReRAM

Time: Wednesday, 10:30 - 10:48

Keywords: Memristor, ReRAM, Pulse Programming, Pulsed Neural Networks

Mohamad Moner Al Chawa (Technische Universität Dresden), Ronald Tetzlaff (TU Dresden), Christos Tjortjis (International Hellenic University), Stavros G. Stavrinides (International Hellenic University), Carol de Benito (Universitat Illes balears) and Rodrigo Picos (Universitat de les Illes Balears).

Abstract

In this work, we present a compact memristor model for bipolar neuromorphic ReRAM devices. The proposed model focuses on a behavioural high level description of the device, and it reproduces some of the most important characteristics (i.e. conductance, energy dissipation), using the number of pulses as the input variable instead of any electrical . Its functionality is shown by using it to model the behavior of three different ReRAM devices that were fabricated and measured at the CNR-IMM, Agrate Brianza. Considering a train of identical pulses as an input voltage signal consisting of pulses and where m is the pulse number. The conductance during depression or potentiation can be described.

REGULAR SESSION 5: MEMRISTOR AND RRAM TECHNOLOGIES

CHAIR : CHRISTOF TEUSCHER

On-Chip Optimization and Deep Reinforcement Learning in Memristor Based Computing

Time: Wednesday, 10:48 - 11:06

Keywords: Reinforcement learning, Memristor, Online learning, In-memory computing, Analog computing

Shahanur Alam (University of Dayton), Chris Yakopcic (University of Dayton) and Tarek Taha (University of Dayton).

Abstract

Reinforcement learning (RL) has shown its viability to learn when an agent interacts continually with the environment to optimize a policy. This work presents a memristor-based deep reinforcement learning (Mem-DRL) system for on-chip training, where the learning process takes place in a dynamic cartpole environment. Memristor device variability is taken into account to make the study more realistic. The proposed system utilized an analog ReLu module to reduce analog to digital converter usage. The analog Mem-DRL system consumed 192 times less energy than an optimized digital FP16 computing system. Mem-DRL computed 9.27 GOPS and exhibited an energy efficiency of 23.8 TOPS/W.

Robust Ex-situ Training of Memristor Crossbar-based Neural Network with Limited Precision Weights

Time: Wednesday, 11:06 - 11:24

Keywords: memristor crossbar, neural network, ex-situ training, sneak path current, limited precision

Raqibul Hasan (Halic University).

Abstract

Memristor crossbar-based neural networks perform parallel operation in the analog domain. Ex-situ training approach needs to program the predetermined resistance values in the memristor crossbar. Because of the stochasticity of the memristor devices, programming a memristor needs to read the device resistance value iteratively. Reading a single memristor in a crossbar (without isolation transistor) is challenging due to the sneak path current. Programming a memristor in a crossbar to either RON or ROFF state is relatively straightforward. A neural network implemented using higher precision weights provides higher classification accuracy compared to a Ternary Neural Network (TNN). This paper demonstrates the implementation of memristor-based neural networks using only the two resistance values (RON, ROFF). At the same time, it achieves higher weight precision. The experimental result shows that the proposed higher precision synapses are easy to program and provide better classification accuracy compared to a TNN.

REGULAR SESSION 5: MEMRISTOR AND RRAM TECHNOLOGIES

CHAIR : CHRISTOF TEUSCHER

Impact of the switching mode on the read noise of ReRAM devices

Time: Wednesday, 11:24 - 11:42

Keywords: ReRAM, VCM, Read noise, Nano-devices

Kristoffer Schnieders (Peter-Grünberg-Institut 7, Forschungszentrum Jülich GmbH, Germany), Stephan Aussen (Peter-Grünberg-Institut 7, Forschungszentrum Jülich GmbH, Germany), Felix Cüppers (Peter-Grünberg-Institut 10, Forschungszentrum Jülich GmbH, Germany), Susanne Hoffmann-Eifert (Peter-Grünberg-Institut 10, Forschungszentrum Jülich GmbH, Germany) and Stefan Wiefels (Peter-Grünberg-Institut 7, Forschungszentrum Jülich GmbH, Germany).

Abstract

Valence change mechanism (VCM)-based memristive devices are interesting candidates for computing in memory and neuromorphic applications. For these devices read noise is a characteristic which is influenced by a variety of factors like the switching mode, namely the area-dependent and the filamentary mode. In this paper we use TiOx -based devices as an example system exhibiting both modes. This allows to only investigate the effect of the modes while excluding other influences. We find that the read noise in the area-dependent mode is lower than for the filamentary mode and that abrupt current jumps are primarily seen for the filamentary mode. This has to be taken into account when choosing the right operation mode for a specific application.

Non-idealities and Design Solutions for Analog Memristor-Based Content-Addressable Memories

Time: Wednesday, 11:42 - 12:00

Keywords: n-Memory computing, Content-Addressable Memory, Memristive Devices, Memristive Circuits, Neuromorphic

Paul-Philipp Manea (PGI-14, Forschungszentrum and RWTH Aachen Univerity), Chirag Sudarshan (PGI-14, Forschungszentrum Jülich), Felix Cüppers (PGI-7, Forschungszentrum Jülich) and John Paul Strachan (PGI-14, Forschungszentrum and RWTH Aachen Univerity).

Abstract

Memristor-based analog Content Addressable Memories (aCAMs) offer robust parallel pattern look-up capabilities, significantly enhancing the scope of In-Memory Computing applications. This paper presents challenges of these analog circuits, which may occur during the inference, and proposes solutions to overcome them. Precisely, we investigate the impact of temperature-dependent behavior, CMOS process variations and memristor telegraph read noise. We demonstrate that the most challenging issue affecting memristors analog computing applications, namely read noise, is not a significant problem in aCAM. We introduce a framework that accounts for these combined distortions to define variability-aware aCAM windows and estimate the bit resolution of a CAM cell. We study how variations affect the inference accuracy of the IRIS classification dataset using our novel torchCAM model. We introduce a streamlined aCAM design featuring a memristor comparator for simplified input-to-reference comparison and a novel cell architecture with two symmetrical memristor comparator units.

REGULAR SESSION 5: MEMRISTOR AND RRAM TECHNOLOGIES

CHAIR : CHRISTOF TEUSCHER

An RRAM-based PUF with Adjustable Programmable Voltage and Multi-Mode Operation

Time: Wednesday, 12:00 - 12:18

Keywords: Resistive random access memory, physical unclonable function, configurable PUF, logic in memory (LiM)

Yijun Cui (Nanjing University of Aeronautics and Astronautics), Jiang Li (Nanjing University of Aeronautics and Astronautics), Chongyan Gu (Queen's University Belfast), Chenghua Wang (Nanjing University of Aeronautics and Astronautics) and Weiqiang Liu (Nanjing University of Aeronautics and Astronautics).

Abstract

The resistive random access memory (RRAM) is one of the promising technology based solutions for energy-efficient reconfigurable logic in memory (LiM) designs. In this paper, a Multi-Mode Configurable Physical Unclonable Function (MC-PUF) is proposed for secure RRAM-based LiM applications. The proposed MC-PUF can be configured to different working modes by adjusting the programming voltages of the corresponding RRAM. When the proposed MC-PUF is configured in a weak write mode, it exploits the inherent variations of an RRAM by adjusting the programming voltages to a switching probability of 50%. When the proposed MC-PUF is programmed in a normal reset voltage and configured in a parallel competition mode, it generates a response by selecting two parallel RRAMs. With the same number of RRAMs, the proposed MC-PUF generates more challenge-response pairs (CRPs) compared to conventional designs. The implementation of the MC-PUF on an RRAM crossbar array is presented. The results from both the experiment and simulation demonstrate that the proposed MC-PUF has good uniqueness, high reliability as well as excellent configurability.

Experimental Verification of Uncoupled Memristive Cellular Nonlinear Network by Processing the EDGE Detection Task

Time: Wednesday, 12:18 - 12:36

Keywords: Memristor Cellular Nonlinear Network, HfO2-based memristive device, experimental demonstrator, uncoupled M-CNNs

Yongmin Wang (Peter-Grünberg-Institut 10 & JARA FIT, Forschungszentrum Jülich GmbH), Kristoffer Schnieders (Peter-Grünberg-Institut 7 & JARA FIT, Forschungszentrum Jülich GmbH), Vasileios Ntinas (Faculty of Electrical and Computer Engineering, Technische Universität Dresden), Alon Ascoli (Faculty of Electrical and Computer Engineering, Technische Universität Dresden), Felix Cüppers (Peter-Grünberg-Institut 10 & JARA FIT, Forschungszentrum Jülich GmbH), Susanne Hoffmann-Eifert (Peter-Grünberg-Institut 10 & JARA FIT, Forschungszentrum Jülich GmbH), Stefan Wiefels (Peter-Grünberg-Institut 7 & JARA FIT, Forschungszentrum Jülich GmbH), Ronald Tetzlaff (Faculty of Electrical and Computer Engineering, Technische Universität Dresden), Vikas Rana (Peter-Grünberg-Institut 10 & JARA FIT, Forschungszentrum Jülich GmbH) and Stephan Menzel (Peter-Grünberg-Institut 7 & JARA FIT, Forschungszentrum Jülich GmbH).

Abstract

The Cellular Nonlinear Network (CNN) is a powerful paradigm in analog computing. As pure-CMOS based CNN Universal Machine faces the von Neumann bottleneck, the integration of memristive devices with their non-volatile memory properties is of major interest. These networks are called Memristor-CNNs (M-CNNs). Moreover, the integration of memristors brings richer dynamics into the network, such that M-CNNs are highly suitable for neuromorphic computing tasks. This paper presents the experimental verification of a processing unit of an uncoupled M-CNN design with a valance change mechanism (VCM) based memristor. We outline a simple measurement strategy to study M-CNNs with real-world devices and provide compelling evidence that the results of the M-CNN processing element are stored in a non-volatile manner. This work further offers crucial insights into design considerations of M-CNN networks.

REGULAR SESSION 6: EMERGING TECHNOLOGIES AND NOVEL MATERIALS

CHAIR : STEFAN SLESAZECK

Low power Circuit Design Using Dynamic GDI Technique in CNTFET Technology

Time: Wednesday, 14:45 - 15:03

Keywords: Carbon Nanotube Field Effect Transistor, Gate Diffusion Input, Low Power, Dynamic Logic

Amandeep Singh Rehal (National Institute of Technology Srinagar Jammu & Kashmir).

Abstract

This paper presents low power circuit design using dynamic gate diffusion input (GDI) technology in Carbon nanotube field effect transistor (CNTFET) technology. GDI technique offers low power with fewer transistor counts and less complexity of circuit and CNTFET technology offers low short channel effect (SCE). NAND and XOR gates-based full adder and two-bit multiplier is designed using the GDI technique and performance analysis is done for various parameters namely power consumption, delay, and power delay product (PDP). Results show that NAND gate-based circuits perform better than XOR-based circuits. Also dynamic GDI NAND gate-based circuits accounts for less power with more flexibility as compared to conventional CMOS-based NAND gate circuits.

Optically Controlled Memristor Using Hybrid ZnO Nanorod/Polymer Material

Time: Wednesday, 15:03 - 15:21

Keywords: optical memristor, bipolar switching, multilevel state, hybrid material

Ayoub Jaafar (School of Physics and Astronomy - University of Nottingham) and Neil Kemp (School of Physics and Astronomy - University of Nottingham).

Abstract

ontrolling of resistive switching properties by optical means opens the route to new optoelectronics that can be written optically and read electronically. In this work, we demonstrate optically controlled memristors realized with a hybrid material of vertically aligned zinc oxide nanorods (ZnO NRs) and poly(methyl methacrylate) (PMMA). In addition to electronic switching, the devices are switchable by optical means upon illumination with UV light. The hybrid memristors require no forming step and exhibit multilevel switching behavior achieved by controlling either the DC sweep voltage or the UV light power. The optical memristor exhibits irreversible switching for the Off state, which has an important application in the fabrication of cloned neural networks with pre-trained information. The work provides a promising pathway for the fabrication of simple-to-make and low-cost optoelectronic devices for memory and optically tuned neuromorphic computing applications.

REGULAR SESSION 6: EMERGING TECHNOLOGIES AND NOVEL MATERIALS

CHAIR : STEFAN SLESAZECK

Single Electron Shuttling between N-Donor and Si/ SiO2 Interface at Room Temperature

Time: Wednesday, 15:21 - 15:39

Keywords: Room Temperature, Silicon architecture, Donor, Deep Dopant, Single Electron shuttling, Qubit Operation

Soumya Chakraborty (INDIAN INSTITUTE OF TECHNOLOGY ROORKEE) and Arup Samanta (INDIAN INSTITUTE OF TECHNOLOGY ROORKEE).

Abstract

We theoretically investigate the prospect of room temperature single qubit operation using a single Nitrogen (N) deep donor within Silicon (Si) quantum computer architecture. We quantitatively demonstrate the possible single electron shuttling between an isolated N-deep donor placed within Si matrix and corresponding dopant induced potential well at the Si / SiO2 interface by the interplay of externally applied electric and magnetic fields. Further, we have added a central cell correction potential to the composite Hamiltonian of the system for a robust description of various parameters associated towards the experimental realization of the proposed device. We also have analyzed and theoretically calculated all the external fields and important time scales involved in the process and their feasibility for the experimental purpose. In practice, we have theoretically demonstrated a room temperature single electron shuttling that in turn will cement the high temperature qubit transfer architecture.

Electrical Properties of Proteinoids for Unconventional Computing Architectures

Time: Wednesday, 15:39 - 15:57

Keywords: proteinoids, computing, microspheres

Panagiotis Mougkogiannis (University of the West of England) and Andrew Adamatzky (University of the West of England).

Abstract

Proteinoids are peptide-like molecules that arise from the combination of amino acids in pre-biotic environments. Recent studies have revealed distinctive electrical characteristics of proteinoids, such as the presence of voltage-gated ion channels, electrical switching capabilities, and the ability to modulate conductivity. Proteinoids possess properties that render them highly favourable as fundamental components for unconventional computing architectures inspired by biological systems. This study involved the synthesis of multiple proteinoids and the subsequent characterisation of their electrical properties through the use of impedance measurements. Proteinoids-based computing logic gates were developed through the integration of proteinoids and electrodes. We developed proteinoid neural networks capable of learning fundamental patterns by adjusting the proteinoid conductivity through training stimuli. Additionally, we have shown that a proteinoid mixture displays rudimentary capabilities for learning and memory. Our findings demonstrate the versatility of proteinoids as nanomaterials that can be utilised in innovative and unconventional computing systems. The utilisation of bio-derived electrical properties and self-assembly of proteinoids has the potential to facilitate the development of environmentally friendly and sustainable neuromorphic or evolutionary computing architectures. Our objective is to improve the complexity and performance of proteinoid computing systems for practical use in the future.

REGULAR SESSION 6: EMERGING TECHNOLOGIES AND NOVEL MATERIALS

CHAIR : STEFAN SLESAZECK

Enhanced Switching in Solid Polymer Electrolyte Memristor Devices via the addition of Interfacial Barriers and Quantum Dots

Time: Wednesday, 15:57 - 16:15

Keywords: Memristors, Polymer Electronics, Polyethylene Oxide (PEO), Polymethacrylate (PMA)

Michael Gater (University of Nottingham), Ali Adawi (University of Hull) and Neil Kemp (University of Nottingham).

Abstract

We report on the electrical effects of single and double polymer (polymethacrylate) barriers on polyethylene oxide (PEO) based memristors. The single barrier device with an active layer embedded with WS2 quantum dots is also investigated. The addition of a single PMA barrier yields multi cross point current-voltage hysteresis while the addition of embedded quantum dots removes multi-cross point behavior and shows repeatable uni-polar switching with the device starting in the low resistive state (LRS). The device shows some capability of reversible unipolar to bipolar operation as a function of applied voltage and device rest time. The addition of a double PMA barrier produces a reproducible unipolar switching behavior and a unipolar negative differential resistance behavior at higher voltage operation.

REGULAR SESSION 7:
QUANTUM COMPUTING AND ADVANCED LOGIC

CHAIR : VASILEIOS NTINAS

Towards Faster Reinforcement Learning of Quantum Circuit Optimisation: Exponential Reward Functions

Time: Wednesday, 16:30 - 16:48

Keywords: quantum circuit, optimization, reinforcement learning, reward function

Ioana Moflic (Aalto University, Finland) and Alexandru Paler (Aalto University, Finland).

Abstract

Reinforcement learning optimization of quantum circuits uses an agent whose goal is to maximize the value of a reward function that tells what is correct and what is wrong during the exploration of the search space. It is an open problem how to formulate reward functions that lead to fast and efficient learning. We propose an exponential reward functions which is sensitive to structural properties of the circuit. We benchmark our function on circuits with known optimum depths, and conclude that our function is reducing the learning time and improve the optimization. Our results are a next step towards fast, large scale optimization of quantum circuits.

REGULAR SESSION 7: QUANTUM COMPUTING AND ADVANCED LOGIC

CHAIR : VASILEIOS NTINAS

A Reconfigurable and Machine Learning attack resistant strong PUF based on Arbiter Mechanism and SOT-MRAM

Time: Wednesday, 16:48 - 17:06

Keywords: PUF, reconfiguration, machine learning, SOT-MRAM

Pengbin Li Pengbin Li (beihang University), Zhengyi Hou (beihang University), Hanran Gao Hanran Gao (beihang University), Bi Wang Bi Wang (beihang University) and Zhaohao Wang Zhaohao Wang (beihang University).

Abstract

This paper presents a strong physical unclonable function (PUF) based on the arbiter mechanism and spin orbit torque magnetic random access memory (SOT-MRAM). This proposed PUF can be easily reconfigured, with 2^32 challenge-response pairs (CRPs) generated during each reconfiguration. Meanwhile, the proposed PUF shows a strong resistance against typical machine learning modeling attacks.

Stochastic template in cellular nonlinear networks modeling memristor induced synaptic noise

Time: Wednesday, 17:06 - 17:24

Keywords: Cellular Nonlinear Networks, Noise, Memristive Synapses

Dimitrios Prousalis (Technische Universität Dresden - TU Dresden), Vasileios Ntinas (Faculty of Electrical and Computer Engineering, Technische Universität Dresden), Ioannis Messaris (Technische Universität Dresden), Ahmet Samil Demirkol (IEE-GE, Technical University of Dresden), Alon Ascoli (TU Dresden) and Ronald Tetzlaff (TU Dresden).

Abstract

Noise is one of the most challenging aspects of cellular nonlinear networks adversely affecting their functionality. Existing techniques to addressing the issues posed by noise are based on well-understood noise removal methods that have reached technical maturity and further have the disadvantage of limited success rates. A deeper understanding and modeling of noise dynamics and its origins are required for the efficient identification and resolution of problems in different network applications. The Stochastic template concept in this article can be beneficial in understanding and modeling noise dynamics in cellular nonlinear networks, which is critical for addressing challenges in network applications. In this paper, memristors functioning as synapses introduce noise into networks, and we conduct an initial investigation of a noisy network performing edge detection.

REGULAR SESSION 7: QUANTUM COMPUTING AND ADVANCED LOGIC

CHAIR : VASILEIOS NTINAS

PolyMiR: Polynomial Formal Verification of the MicroRV32 Processor

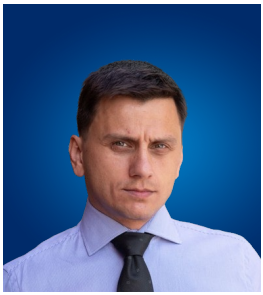
Time: Wednesday, 17:24 - 17:42

Keywords: Polynomial Formal Verification, RISC-V, Multi-cycle processor, Binary Decision Diagrams (BDDs)

Lennart Weingarten (University of Bremen), Kamalika Datta (University of Bremen/DFKI) and Rolf Drechsler (University of Bremen/DFKI).

Abstract

Formal verification techniques ensure completeness as opposed to simulation-based techniques. In general, the process of formal verification is computationally complex, and it is difficult to quantify the exact time and space complexities. Some of the recent works have shown that it is possible to achieve polynomial space and time complexities for verifying specific designs like arithmetic circuits. However, this cannot be directly extended to complex circuits like processors. A recent work has reported a formal verification method for the RISC-V processor with polynomial complexity, where only single-cycle instruction execution was considered and it was computation intensive. This method cannot be directly extended to multi-cycle operations, which are typical of most real processors. This paper introduces an improved data structure leading to Binary Decision Diagram (BDD) based Polynomial Formal Verification (PFV) with support for both single-cycle and multi-cycle operations. We use the MicroRV32 processor as a case study. Our method leads to significant improvement in runtime over the previous method. The entire process of verification can be carried out in polynomial space and time complexities for multi-cycle operations, which is the first such demonstration to the best of our knowledge.



A T-depth two Toffoli gate for 2D square lattice architectures

Time: Wednesday, 17:42 - 18:00

Keywords: Quantum circuit, quantum gate, Toffoli gate, Clifford+T

Alexandru Paler (Aalto University, Finland), Evan Dobbs (The University of Texas at Dallas) and Joseph S. Friedman (The University of Texas at Dallas).

Abstract

We present a novel Clifford+T decomposition of a Toffoli gate. Our decomposition requires no SWAP gates in order to be implemented on 2D square lattices of qubits. This decomposition will enable shallower, more fault-tolerant quantum computations on both NISQ and error-corrected architectures. We present the derivation of the circuit, and illustrate the qubit mapping on a Sycamore-like architecture.

NOTES