NANOARCH 2023 - AGENDA

NANOARCH 2023

Monday, Dec. 18

8:30-9:00	**Registration & Welcome Address**
9:00-10:15	Keynote 1: **Subhasish Mitra** Chair: Ronald Tetzlaff
10:15-10:30	**Coffee break**

RS1: Advanced Computing Architectures and Systems
Chair: Ioannis Messaris

10:30-10:48	A Spatial-Designed Computing-In-Memory Architecture Based on Monolithic 3D Integration for High-Performance Systems Jiaming Li
10:48-11:06	Minimal Design of SiDB Gates: An Optimal Basis for Circuits Based on Silicon Dangling Bonds Jan Drewniok
11:06-11:24	Post-Layout Optimization for Field-Coupled Nanotechnologies Simon Hofmann
11:24-11:42	Memristor-based Network Switching Architecture for Energy Efficient Cognitive Computational Models Saad Saleh
11:42-12:00	LUT-based RRAM Model for Neural Accelerator Circuit Simulation Max Uhlmann
12:00-12:18	Resilience and Precision Assessment of Natural Language Processing Algorithms in Analog In-Memory Computing: A Hardware-Aware Study Amirhossein Parvaresh
12:18-12:36	VLCP: A High-Performance FPGA-based CNN Accelerator with Vector-level Cluster Pruning Shuo Ran
12:36-13:30	**Lunch (incl. Group picture)**
13:30-14:15	Invited Talk: **Hussam Amrouch** Chair: Vasileios Ntinas
14:15-14:45	**Coffee break**
14:45-16:15	**Industry Session** Panelist Talks Chair: Ronald Tetzlaff
16:15-16:30	**Coffee break**
16:30-17:30	**Industry Session** Panel Discussion Chair: Ronald Tetzlaff
17:30-19:00	**Welcome Reception**
19:30-20:30	**Guided City Tour with Stollen Baker Grete**

Tuesday, Dec. 19

8:30-9:00	**Registration**
9:00-10:15	Keynote 2: **Tony Kenyon** Chair: Neil Kemp
10:15-10:30	**Coffee break**
10:30-11:15	Invited Talk: **Karl Leo** Chair: Ronald Tetzlaff

RS2: Neuromorphic Computing and Neural Networks
Chair: Farhad Merchant

11:15-11:33	Towards Temporal Information Processing – Printed Neuromorphic Circuits with Learnable Filters Haibin Zhao
11:33-11:51	Material and Physical Reservoir Computing for Beyond CMOS Electronics: Quo Vadis? Christof Teuscher
11:51-12:09	Non Volatile Operators Emulation Platform Alban Nicolas
12:09-12:27	Neural Network Modeling Bias for Hafnia-based FeFETs Gina Adam
12:27-12:45	Multiplexer Optimization for Adders in Stochastic Computing Sercan Aygun
12:45-13:45	**Lunch**

RS3: Hardware and System Optimizations
Chair: Asal Kiazadeh

13:45-14:03	Reducing the Complexity of Operational Domain Computation in Silicon Dangling Bond Logic Marcel Walter
14:03-14:21	Accurate and Energy-Efficient Stochastic Computing with Van Der Corput Sequences Jonas I Schmidt
14:21-14:39	Heterogeneous Instruction Set Architecture for RRAM-enabled In-memory Computing Hosui Zhou
14:39-14:57	A Robust Time-based Error-Proofing Readout Scheme for MRAM Qianlei Qu
15:00-15:15	**Coffee break**

RS4: Novel Technologies and Future Networks
Chair: Gina Adam

15:15-15:33	Hyper Dimensional Computing with Ferroelectric Tunneling Junctions Stefan Slesazeck
15:33-15:51	Spin Wave Threshold Logic Gates Arne Van Zeghroeck
15:51-16:09	Exploring Multi-Valued Logic and Its Application in Emerging Post-CMOS Technologies Farhad Merchant
16:09-16:27	Concept paper on novel radio frequency resistive switches Asal Kiazadeh
16:30-16:45	**Coffee break**
16:45-17:30	Invited Talk: **Gianaurelio Cuniberti** Chair: Neil Kemp
19:00-23:00	**Gala Dinner**

Wednesday, Dec. 20

8:30-9:00	**Registration**
9:00-10:15	Tutorial Session: **Fernando Corinto** **Georgios Ch. Sirakoulis** Chair: Alon Ascoli
10:15-10:30	**Coffee break**

RS5: Memristor and RRAM Technologies
Chair: Christof Teuscher

10:30-10:48	A Behavioural Compact Model for Programmable Neuromorphic ReRAM M. Moner Al Chawa
10:48-11:06	On-Chip Optimization and Deep Reinforcement Learning in Memristor Based Computing Tarek Taha
11:06-11:24	Robust Ex-situ Training of Memristor Crossbar-based Neural Network with Limited Precision Weights Ragibul Hasan
11:24-11:42	Impact of the switching mode on the read noise of ReRAM devices Kristoffer Schnieders
11:42-12:00	Non-idealities and Design Solutions for Analog Memristor-Based Content-Addressable Memories Paul-Philipp Manea
12:00-12:18	An RRAM-based PUF with Adjustable Programmable Voltage and Multi-Mode Operation Yijun Cui
12:18-12:36	Experimental Verification of Uncoupled Memristive Cellular Nonlinear Network by Processing the EDGE Detection Task Yongmin Wang
12:36-13:30	**Lunch**
13:30-14:15	Invited Talk: **Erika Covi** Chair: Fernando Corinto
14:15-14:45	**Coffee break**

RS6: Emerging Technologies and Novel Materials
Chair: Stefan Slesazeck

14:45-15:03	Low power Circuit Design Using Dynamic GDI Technique in CNTFET Technology Amandeep Singh Rehal
15:03-15:21	Optically Controlled Memristor Using Hybrid ZnO Nanorod/Polymer Material Ayoub Jaafar
15:21-15:39	Single Electron Shuttling between N-Donor and Si/SiO2 Interface at Room Temperature Soumya Chakraborty
15:39-15:57	Electrical Properties of Proteinoids for Unconventional Computing Architectures Panagiotis Mougkogiannis
15:57-16:15	Enhanced Switching in Solid Polymer Electrolyte Memristor Devices via the addition of Interfacial Barriers and Quantum Dots Michael Gater
16:15-16:30	**Coffee break**

RS7: Quantum Computing and Advanced Logic
Chair: Vasileios Ntinas

16:30-16:48	Towards Faster Reinforcement Learning of Quantum Circuit Optimisation: Exponential Reward Functions Ioana Moflic
16:48-17:06	A Reconfigurable and Machine Learning attack resistant strong PUF based on Arbiter Mechanism and SOT-MRAM Zhengyi Hou
17:06-17:24	Stochastic template in cellular nonlinear networks modeling memristor induced synaptic noise Dimitrios Prousalis
17:24-17:42	PolyMIR: Polynomial Formal Verification of the MicroRV32 Processor Lennart Weingarten
17:42-18:00	A T-depth two Toffoli gate for 2D square lattice architectures Alexandru Paler
18:00-18:15	**Farewell & Best Paper Award Ceremony**

TECHNISCHE UNIVERSITÄT DRESDEN

FAKULTÄT ELEKTROTECHNIK UND INFORMATIONSTECHNIK

DFG Deutsche Forschungsgemeinschaft

acm

CMC Chua Memristor Center