Call for Papers

NANOARCH 2012

8th ACM/IEEE International Symposium on Nanoscale Architectures

July 4-6, 2012, Amsterdam, The Netherlands

http://nanoarch.org

NANOARCH is the annual cross-disciplinary forum for the discussion of novel post-CMOS and advanced nanoscale CMOS directions. The symposium seeks papers on innovative ideas for solutions to the principal challenge facing integrated electronics in the 21st century – how to design, fabricate, and integrate nanosystems to overcome the fundamental limitations of CMOS. In particular, such systems could (1) contain unconventional nanodevices with unique capabilities, including directions beyond simple switches, (2) introduce new logic and memory concepts, (3) involve novel circuit styles, (4) introduce new concepts for computing, (5) reconfigure and/or mask faults at much higher rates than in CMOS, (6) involve new paradigms for manufacturing, and (7) rethink the methodologies and design tools involved.

This 8th symposium introduces, for the first time, several new exciting special sessions (e.g., Nano-CMOS, Reliability) and opportunities for interaction. In addition to Regular papers presenting original techniques/directions, it invites the community to also submit Nanofabric Progress Updates giving a progress update of their nanofabrics directions to date across devices, circuits, architecture, and manufacturability aspects – e.g., 2D/3D nanowire, spintronics, memristor, CNT, graphene, FinFETs, and QCA based directions. In addition, Crosscut papers are invited from the broader nanotechnology community to highlight promising nanomaterial, nanodevice, nanomanufacturing, and integration ideas with application potential in nanoscale architectures.

Example **topics** (both theoretical and experimental) of interest include (but are not limited to):

- Novel nanodevices and manufacturing/integration ideas with a focus on nanoarchitectures
- Nanoelectronic circuits, nanofabrics, computing paradigms and nanoarchitectures
- Paradigms and nanoarchitectures for computing with unpredictable devices
- Reliability aware computing
- 3D hybrid nanoarchitectures
- 2D/3D/hybrid nanodevice integration and manufacturing, with defect and fault tolerance
- Nanodevice and nanocircuit models, methodologies and computer aided design tools
- Fundamental limits of computing at the nanoscale

Important Dates

- **Paper submission: April 10, 2012**
- Acceptance notification: May 10, 2012
- Early registration deadline: June 1, 2012
- Final version: June 1, 2012

Authors are invited to submit papers of 4-8 pages in length for the Regular, nano CMOS, Reliability, Nanofabrics Progress Updates, and Crosscut Sessions. The electronic submission will be considered evidence that upon acceptance, the author(s) will present their paper at the symposium. Accepted papers will be included in the Symposium Proceedings, published in IEEE Xplore and will be considered for the NANOARCH Best Paper Awards. Extended versions of the most exciting papers will be published (subject to a further review process) in a NANOARCH 2012 Special Session in IEEE Transactions on Nanotechnology.

GENERAL CHAIR: Csaba Andras Moritz, UMass in Amherst, USA
PROGRAM CHAIR: Sorin Cotofana, Delft University of Technology, The Netherlands
PROGRAM CO-CHAIR: Jaques-Olivier Klein, University Paris Sud, France