Program

NANOARCH 2012

8th ACM/IEEE International Symposium on Nanoscale Architectures

July 4-6, 2012, Amsterdam, The Netherlands

http://nanoarch.org

WEDNESDAY
JULY 4, 2012

9:00 – 9:30 **Coffee & Refreshments**

9:30 **Introduction**

9:45 **Keynote: Majorana Fermions in Semiconductor Nanowires**
***Leo Kouwenhoven*, Kavli Institute of NanoScience, Delft, The Netherlands**

10:45 – 13:15 **Session 1 – Ambipolar and Double Gate based Architectures**
Chair: Costin Anghel, ISEP, Paris, France

10:45 **Ambipolar Circuits for Analog, Mixed-Signal, and RF Applications** – *Kartik Mohanram, Xuebei Yang, Guanxiong Liu, Masoud Rostami, and Alexander Balandin*, University of Pittsburgh, USA

11:15 **Ambipolar Double Gate CNTFETs based Reconfigurable Logic Cells** – *Kotb Jabeur, Ian O'Connor, Sébastien Le Beux, David Navarro,* Ecole Centrale de Lyon- Lyon Institute of Nanotechnology - University of Lyon, France

11:30 **Low-Power Design Technique with Ambipolar Double Gate Devices** – *Kotb Jabeur, Ian O'Connor, David Navarro, Sebastien Le Beux,* Ecole Centrale de Lyon- Lyon Institute of Nanotechnology - University of Lyon, France

11:45 – 13:15 **Lunch (Included)**

13:15 – 14:15 **Poster Session 1 (5 min. Oral presentation per poster)**
Chair: Garrett Rose, Air Force Research Laboratory, USA

13:15 **Gate-Level Modeling for CMOS Circuit Simulation with Ultimate FinFETs** – *Nicolas Chevillon, Morgan Madec and Christophe Lallement,* University of Strasbourg, France

13:20 **Design Exploration of Ultra-Low Power Non-volatile Memory based on Topological Insulator** – *Yuhao Wang and Hao Yu,* Nanyang Technological University, Singapore

13:25 **A Conventional Design Of CLB Implementation for an FPGA In Quantum-dot Cellular Automata (QCA)** – *Moein Kianpour and Reza Sabbaghi*, IAU, Iran

13:30 **Introducing OVP Awareness to Achieve an Efficient Permanent Defect Locating** – *Tanvir Ahmed, Jun Yao, and Yasuhiko Nakashima,* Nara Institute of Science and Technology, Japan

13:35 **Irreversibility Induced Density Limits and Logical Reversibility in Nanocircuits** – *Ismo Hänninen and Jarmo Takala,* Tampere University of Technology, Finland

13:40 – 14:15 **Poster Viewing & Discussion**

14:15 – 15:45 **Session 2 – Ambipolar, Double Gate based Logic and Memories**
Chair: Christof Teuscher, Portland State University, USA

14:15 **Process/Design Co-optimization of Regular Logic Tiles for Double-Gate Silicon Nanowire Transistors** – *Shashikanth Bobba, Pierre-Emmanuel Gaillardon, Jian Zhang, Michele De Marchi, Davide Sacchetto, Yusuf Leblebici and Giovanni De Micheli,* EPFL, Switzerland

14:45 **Ambipolar Independent Double Gate FET Logic** – *Ian O'Connor, Kotb Jabeur, Sébastien Le Beux and David Navarro,* Ecole Centrale de Lyon, France

15:00 **Ternary Volatile Random Access Memory based on Heterogeneous Graphene-CMOS Fabric** – *Santosh Khasanvis, K. M. Masum Habib, Mostafizur Rahman, Pritish Narayanan, Roger K. Lake and Csaba Andras Moritz*, University of Massachusetts Amherst, USA

15:15 **Macromodeling a Phase Change Memory (PCM) Cell by HSPICE** – Pilin Junsangsri, Jie Han, Fabrizio Lombardi, Northeastern University, USA

15:45 – 16:05 **Coffee & Refreshments**

16:05 – 17:35 **Session 3 – Memristor and Crossbar Architectures**
Chair: Pierre-Emmanuel Gaillardon, EPFL, Switzerland

16:05 **Crossbar Architecture Based on 2R Complementary Resistive Switching Memory Cell** – *W.S. Zhao, Y.Zhang, J.O Klein, D. Querlioz, D. Chabi, D. Ravelosona, C. Chappert, J.M. Portal, M. Bocquet, H. Aziza, D.Deleruyelle, and C. Muller,* IM2NP, IMT Tehcnopole de Chateau Gombert, France

16:35 **A Monte Carlo Analysis of a Write Method used in Passive Nanoelectronic Crossbars** – *Arne Heittmann, Tobias G. Noll,* RWTH Aachen, Germany

17:05 **RRAM-based FPGA for "Normally Off, Instantly On" Applications** – *Ogun Turkyilmaz, Santhosh Onkaraiah, Marina Reyboz, Fabien Clermidy, Hraziia, Costin Anghel, Jean-Michel Portal, and Marc Bocquet*, CEA, LETI, France

17:35 **End of First Day**

THURSDAY
JULY 5, 2012

9:00 – 9:30 **Coffee & Refreshments**

9:30 – 11:00 **Session 4 – Reliability and Fault Tolerance**
Chair: Antonio Rubio, UPC, Barcelona, Spain

9:30 **Statistical Reliability Analysis of NBTI Impact on FinFET SRAMs and Mitigation Technique Using Independent-Gate Devices** – *Yao Wang, Sorin Cotofana, and Liang Fang*, Delft University of Technology, the Netherlands

10:00 **A Markovian, Variation-Aware Circuit-Level Aging Model** – *N. Cucu Laurenciu and S.D. Cotofana,* Technical University of Delft, The Netherlands

10:30 **Zero-Performance-Overhead Online Fault Detection and Diagnosis in 3D Stacked Integrated Circuits** – *Saleh Safiruddin, Mihai Lefter, Demid Borodin, George Voicu, Sorin Dan Cotofana,* TU Delft, The Netherlands

10:45 **Design and Reliability Analysis of Multiple Valued Logic Gates using Carbon Nanotube FETs** – *Jinghang Liang, Linbin Chen, Jie Han and Fabrizio Lombardi,* University of Alberta, Canada

11:00 – 12:00 **Poster Session 2 (5 min. Oral presentation per poster)**
Chair: Garrett Rose, Air Force Research Laboratory, USA

11:00 **Emitter-Coupled Spin-Transistor Logic** – *Joseph S. Friedman, Yehea I. Ismail, Gokhan Memik, Alan V. Sahakian, and Bruce W. Wessels*, Northwestern University, USA

11:05 **Room Temperature Double Gate Single Electron Transistor based Standard Cell Library** – *Mohamed Amine Bounouar, Arnaud Beaumont, Khalil El Hajjam, Francis Calmon, Dominique Drouin*, Université de Sherbrooke, Canada

11:10 **Cell Design and Comparative Evaluation of a 1T Memristor-based Memory** – *Vikas Sakode, Jie Han, and Fabrizio Lombardi*, Northeastern University, USA

11:15 **ToPoliNano: Nanoarchitecture Design Made Real** – *S. Frache, D. Chiabrando, M. Graziano, F. Riente, G. Turvani, and M. Zamboni*, Politecnico di Torino, Italy

11:20 **A Novel Write-Scheme for Data Integrity in Memristor-Based Crossbar Memories** – *Angelo Giuseppe Ruotolo, Marco Ottavi, Salvatore Pontarelli, and Fabrizio Lombardi*, Univesity of Rome «Tor Vergata», Italy

11:25 – 12:00 **Poster Viewing & Discussion**

12:00 – 13:15 **Lunch (Included)**

13:15 – 14:45 Session 5 – SET, Quantum and Spintronics Computing
Chair: Fabrizio Lombardi, Northeastern University, USA

13:15 **Stigmergic Search with Single Electron Tunneling Technology based Memory Enhanced Hubs** – *Saleh Safiruddin, Ferdinand Peper, and Sorin Cotofana*, TU Delft, The Netherlands

13:45 **Synthesis of Topological Quantum Circuits** – *Alexandru Paler, Simon Devitt, Kae Nemoto, and Ilia Polian*, University of Passau, Germany

14:00 **Spintronic Threshold Logic Array - A Compact, Low Leakage, Non-Volatile Gate Array Architecture** – *Nishant Nukala, Niranjan Kulkarni, and Sarma Vrudhula*, Arizona State University, USA

14:30 **Spin Wave Nanofabric Update** – *J. G. Alzate, P. Upadhyaya, M. Lewis, J. Nath, Y. T. Lin, K. Wong, S. Cherepov, P. Khalili Amiri, K. L. Wang, J. Hockel, G. P. Carman*, UCLA; *J. Zhu, Y-J Chen, I. N. Krivorotov*, UC – Irvine; *J. Katine*, Hitachi GST Research Center; *J. Langer*, Singulus Technologies AG; *P. Shabadi, S. Khasanvis, S. Narayanan, C. A. Moritz,* UMass Amherst; and *A. Khitun*, University of California – Riverside, USA

14:45 Keynote: Technology Innovation and Supporting Mechanisms in Europe
***Andreas Wild*, ENIAC Joint Undertaking**

15:45 – 16:05 Coffee & Refreshments

16:05 – 17:35 Session 6 – Neural Computing
Chair: Ian O'Connor, Lyon Institute of Nanotechnology, France

16:05 **Bioinspired Networks with Nanoscale Memristive Devices that Combine the Unsupervised and Supervised Learning Approaches** – *D. Querlioz, W. S. Zhao, P. Dollfus, J.-O. Klein, O. Bichler, and C. Gamrat,* Univ. Paris-Sud, France

16:35 **Ultra Low Energy Analog Image Processing Using Spin Based Neurons** – *Mrigank Sharad, Charles Augustine, Georgios Panagopoulos, and Kaushik Roy*, Purdue University, USA

17:05 **RRAM-based Adaptive Neural Logic Block for Implementing Non-Linearly Separable Functions in a Single Layer** – *Michael Soltiz, Cory Merkel, Dhireesha Kudithipudi, and Garrett Rose*, Rochester Institute of Technology, USA

17:20 **Memrisor-based Reservoir Computing** – *Manjari Kulkarni and Christof Teuscher,* Portland State University, USA

17:35 Closing Remarks

17:40 End of Technical Program

FRIDAY
JULY 6, 2012

09:45 Departure from the Movenpick Hotel, Amsterdam

10:45 – 11:45 Guided tour of Edam / 1 hour In two groups of 25 persons

13:00 – 14:00 Dutch style lunch (Includes soup, two sandwiches and coffee or tea)

14:00 – 14:30 Photo in Volendam costume

14:30 – 16:30 Visit to Marken (Round trip by boat / guide)

16:30 – 17:30 Guided tour Volendam

17:30 – 19:00 Dinner on the dike (Buffet)

19:00 Departure from Volendam towards the Movenpick Hotel, Amsterdam