NANOARCH 2013 Advance Program

Monday July 15th

8:30 AM	**Breakfast**
9:00 AM	**Welcome and Introduction**
	C.A. Moritz, R. Karri, K. Roy & S. Bhunia
9:15 AM	**Opening Keynote** ***Session Chair: Kaushik Roy, Purdue U., USA***
	Title: *Energy-Efficient Computing in Nanoscale CMOS: Challenges and Opportunities* ***Vivek De, Ph.D*** *Intel Fellow and Director of Circuit Technology Research, Intel Corporation*
10:15 AM	**Session I – Memristor: Novel Applications**
	Chair: Fabrizio Lombardi, Northeastern University, USA
10:15-10:35	**Variation-tolerant Computing with Memristive Reservoirs** *Jens Bürger and Christof Teuscher* Portland State University, USA
10:35-10:55	**Design Exploration Methodology for Memristor-Based Spiking Neuromorphic Architectures with the Xnet Event-Driven Simulator** *Olivier Bichler, Damien Querlioz, David Roclin and Christian Gamrat* CEA-LETI, France
10:55-11:15	**Doped HfO2 based Nanoelectronic Memristive Devices for Self-Learning Neural Circuits and Architecture** *Saptarshi Mandal, Branden Long, Ammaarah El-Amin and Rashmi Jha* U. of Toledo, USA
11:15 AM	**Break**
11:30 AM	**Session II – Concept Papers: Computing Paradigm**
	Chair: Jacques-Olivier Klein, Univ. Paris-Sud, France
11:30-11:40	**Digital-to-Analog and Analog-to-Digital Conversion with Metal Oxide Memristors for Ultra-Low-Power Computing** *Ligang Gao, Farnood Merrikh-Bayat, Fabien Alibart, Brian Hoskins, Kwang-Ting Cheng and Dmitri Strukov* U. of California, Santa Barbara, USA
11:40-11:50	**Nanowire Field-Programmable Computing Platform** *Santosh Khasanvis, Mostafizur Rahman, Prasad Shabadi, Pritish Narayanan, Hyung Suk Yu, Chi On Chui and Csaba Andras Moritz* U. of Massachusetts Amherst, USA
11:50-12:00	**MRAM-based Logic Array for Large-Scale Non-Volatile Logic-in-Memory Applications** *Hiwa Mahmoudi, Thomas Windbacher, Viktor Sverdlov and Siegfried Selberherr* Institute for Microelectronics, TU Vienna
12:00-12:10	**Energy Efficient Computing Using Coupled Dual-Pillar Spin Torque Nano Oscillators** *Mrigank Sharad, Karthik Yogendra and Kaushik Roy* Purdue U., USA
12:10-12:20	**Design Methodologies for High Density Domain Wall Memory** *Swaroop Ghosh* U. of South Florida, USA
12:20-12:30	**Embedded Processors based on Spin Wave Functions (SPWFs)** *Santosh Khasanvis, Sankara Narayanan Rajapandian, Prasad Shabadi, Jiajun Shi and Csaba Andras Moritz* U. of Massachusetts Amherst, USA
12:30 PM	**Lunch**

1:45 PM	**Session III – Concept Papers: Devices & Circuits**
	Chair: Pierre-Emmanuel Gaillardon, EPFL, Switzerland
1:45-1:55	**Pulsed READ in Spin Transfer Torque (STT) Memory Bitcell for Lower READ Disturb** *Arijit Raychowdhury* Georgia Institute of Technology, USA
1:55-2:05	**Novel MTJ-Based Shift Register for Non-Volatile Logic Applications** *Thomas Windbacher, Hiwa Mahmoudi, Viktor Sverdlov and Siegfried Selberherr* Institute for Microelectronics, TU Wien, Austria
2:05-2:15	**A Pseudo-weighted Sensing Scheme for Memristor Based Cross-point Memory** *Zhijie Chen, Lu Zhang, Xiuyuan Bi and Hai Li* U. of Pittsburgh, USA
2:15-2:25	**Reading Spin-Torque Memory with Spin-Torque Sensors** *Mrigank Sharad, Rangharajan Venkatesan, Xuanyao Fong, Anand Raghunathan and Kaushik Roy* Purdue U., USA
2:25-2:35	**Charge distribution in a molecular QCA wire based on bis-ferrocene molecules** *Azzurra Pulimeno, Mariagrazia Graziano, Ruiyu Ruiyu, Danilo Demarchi and Gianluca Piccinini* Politecnico di Torino, Italy
2:35-2:45	**Nanomechanical Non-Volatile Memory for Computing at Extreme** *Vaishnavi Ranganathan, Tina He, Srihari Rajgopal, Mehran Mehregany, Philip X.-L. Feng, and Swarup Bhunia* Case Western Reserve U., USA
2:45 PM	**PANEL – *What Lies in Our (Nanoelectronic) Future?***
	Chair: Arijit Raychowdhury, Georgia Institute of Technology, USA ***Panelists:*** ***Dr. Roger Howe, Stanford University, USA*** ***Dr. Hillery Hunter, IBM T. J. Watson Research Center, USA*** ***Dr. Philip Kim, Columbia University, USA*** ***Dr. Jacques-Olivier Klein, University of Paris-Sud, FRANCE*** ***Dr. Garrett Rose, Air Force Research Laboratory, USA***
4:00 PM	**Tea Break** **Poster Presentation for All Concept Papers**
4:30 PM	**Session IV – Emerging Devices - I**
	Chair: Swaroop Ghosh, U. of South Florida, USA
4:30-4:50	**SATSoT: A Methodology to Map Controllable-Polarity Devices on a Regular Fabric Using SAT** *Catherine Gasnier, Pierre-Emmanuel Gaillardon and Giovanni De Micheli* LSI – EPFL, Switzerland
4:50-5:10	**Foundations of Memristor Based PUF Architectures** *Garrett Rose, Nathan Mcdonald, Lok-Kwong Yan, Bryant Wysocki and Karen Xu* Air Force Research Laboratory, USA
5:10-5:30	**Automatic Place & Route of Nano-Magnetic Logic Circuits** *Marco Vacca, Stefano Frache, Mariagrazia Graziano, Luca Di Crescenzo, Fabrizio Cairo and Maurizio Zamboni* Politecnico di Torino, Italy
5:30 PM	**End of Technical Session on the First Day**
7:00PM	**Banquet / Dinner**

Tuesday July 16th

8:30 AM	**Breakfast**
9:00 AM	**Keynote** ***Session Chair: Swarup Bhunia, Case Western Reserve U., USA***
	Title: *Nanoelectromechanical (NEM) relays for low-power, adaptive digital systems* ***Roger T. Howe, Ph.D.*** *William E. Ayer Professor of Eng, Stanford U., USA; Director, National Nanotechnology Infrastructure Network*
10:10 AM	**Session V – Resistive Memory and Logic**
	Chair: Wenjing Rao, U. of Illinois at Chicago, USA
10:10-10:30	**Understanding the Impact of Diode Parameters on Sneak Current in 1Diode 1ReRAM Crossbar Architectures** *Yibo Li, Branden Long, Saptarshi Mandal, Wenbo Chen and Rashmi Jha* U. of Toledo, USA
10:30-10:50	***Analytical Study of Complementary Memristive Synchronous Logic Gates*** *Jean-Michel Portal, Mathieu Moreau, Marc Bocquet, Hassen Aziza, Damien Deleruyelle, Christophe Muller, Yue Zhang, Erya Deng, Jacques-Olivier Klein, Damien Querlioz, Dafine Ravelosona, Claude Chappert and Weisheng Zhao* M2NP - Aix Marseille University, France
10:50-11:10	**Content-aware Encoding for Improving Energy Efficiency in Resistive Random Access Memory** *Hadi Hajimiri, Prabhat Mishra, Swarup Bhunia, Branden Long, Yibo Li, and Rashmi Jha* U. of Florida, USA
11:10 AM	**Break**
11:30 AM	**Session VI – Crosscuts**
	Chair: Rashmi Jha, U. of Toledo, USA
11:30-11:50	**Schottky-Barrier-Type Graphene Nano-Ribbon Field-Effect Transistors: A Study on Compact Modeling, Process Variation, and Circuit Performance** *Ying-Yu Chen, Amit Sangai, Morteza Gholipour and Deming Chen* U. of Illinois at Urbana-Champaign, USA
11:50-12:10	**A PCM-based TCAM cell using NDR** *Fabrizio Lombardi, Hao Wu and Jie Han* Northeastern U., USA
12:10-12:30	**Stochastic Neuron Design using Conductive Bridge RAM** *Giorgio Palma, Manan Suri, Damien Querlioz, Elisa Vianello and Barbara De Salvo* CEA-LETI, France
12:30 PM	**Lunch**
1:45 PM	**Social Event (Guided tour of American Museum of Natural History)**
2:30 PM	*Tour guide meets everyone at the Rose Center Will Call desk of the Museum*

Wednesday July 17th

8:30 AM	**Breakfast**
9:00 AM	**Session VII – Reliability & Energy-Aware Design**
	Chair: Christof Teuscher, Portland State U., USA
9:00-9:20	**Throughput-Dissipation Tradeoff in Partially Reversible Computing: A Case Study**
	Kyle Stearns and Neal Anderson
	U. of Massachusetts Amherst, USA
9:20-9:40	**Extending the Fundamental Error Bounds for Asymmetric Error Reliable Computation**
	Nivard Aymerich and Antonio Rubio
	UPC Barcelona Tech, Spain
9:40-10:00	**Proactive Thermal Management Using Memory Based Computing**
	Hadi Hajimiri, Mimonah Al Qathrady and Prabhat Mishra
	U. of Florida, USA
10:00 AM	**Session VIII – 3D Integration**
	Chair: Naghmeh Karimi, Polytechnic Institute of New York U., USA
10:00-10:20	**A Cellular Architecture for Self-Assembled 3D Computational Devices**
	Nick Macias, S. Pandey, A. Deswandikar, C. K. Kothapalli, C. K. Yoon, D. H. Gracias and Christof Teuscher
	Portland State University, USA
10:20-10:40	**Towards Heterogenous 3D-Stacked Reliable Computing with von Neumann Multiplexing**
	George R. Voicu and Sorin Cotofana
	Delft University of Technology, Netherlands
10:40-11:00	**On the Impact of 3D Integration on High-Throughput Sensor Information Processing: A Case Study with Image Sensing**
	Denny Lie, Kwanyeob Chae and Saibal Mukhopadhyay
	Georgia Institute of Technology, USA
11:00 AM	**Break**
11:10 AM	**Session IX – Emerging Devices - II**
	Chair: Prabhat Mishra, U. of Florida, USA
11:10-11:30	**Experimental Prototyping of beyond-CMOS Nanowire Computing Fabrics**
	Mostafizur Rahman, Pritish Narayanan, Santosh Khasanvis, John Nicholson and Csaba Andras Moritz
	U. of Massachusetts Amherst, USA
11:30-11:50	**Impact of PCM Resistance-Drift in Neuromorphic Systems and Drift-Mitigation Strategy**
	Manan Suri, Daniele Garbin, Olivier Bichler, Damien Querlioz, Dominique Vuillaume, Christian Gamrat and Barbara Desalvo
	CEA-LETI, France
11:50-12:10	**Effect of potential disorder on shot noise suppression in nanoscale devices**
	Paolo Marconcini
	Universita' di Pisa, Italy
12:10-12:30	**Design of 8T-Nanowire RAM Array**
	Vikram Suresh, Akshaya Shanmugam, Lekshmi Krishnan, Avinash Bijjal, Mostafizur Rahman and Andras Moritz
	U. of Massachusetts Amherst, USA
12:30 PM	**Lunch | Student Award Announcement | Closing Remarks**
1:45 PM	**End of Technical Program**