Call for Papers

NANOARCH 2013

9th ACM/IEEE International Symposium on Nanoscale Architectures

July 15-17, 2013, New York City, USA

http://www.nanoarch.org

NANOARCH is the annual cross-disciplinary forum for the discussion of novel post-CMOS and advanced nanoscale CMOS technology, circuits, architectures and systems. The symposium seeks papers on innovative ideas for solutions to the principal challenge facing integrated electronics in the 21st century – how to design, model, fabricate, and integrate nanosystems to overcome the fundamental limitations of CMOS. Such systems could (1) contain unconventional nanodevices with unique capabilities, e.g., nanowires, nanotubes, graphene, resistive and spin-based devices, (2) introduce new logic and memory circuit styles, (3) introduce new concepts on computing model and architecture to address the energy, reliability and security issues, (4) reconfigure and/or mask faults at much higher rates than in CMOS, (5) involve new paradigms for manufacturing, (6) effectively integrate nanosensors with nanoelectronics, and (7) rethink the methodologies and design tools involved.

This 9th symposium will incorporate several exciting special sessions (e.g., beyond charge-based computing, benefits and challenges with emerging memory devices, and nanoelectronics for biomedical systems) and opportunities for interaction. In addition to ***Regular Papers*** (of up to 6 pages in length), we also invite 2-page ***Concept Papers*** in the area of nanofabrication, nano-computing, and emerging applications of nanosystems for presentation in Special Sessions. These concept papers would present less-developed but radical and highly innovative work.

Example topics (both theoretical and experimental) of interest include (but are not limited to):

- Novel nanodevices and manufacturing/integration ideas with a focus on nanoarchitectures
- Nanoelectronic circuits, nanofabrics, computing paradigms and nanoarchitectures
- Paradigms and nanoarchitectures for computing with unpredictable devices
- Nanoscale security primitives, nanoforensics and nanoscale hardware-based security protocols
- Security threats on nanosystems
- Energy-efficient, reliable and secure nano-computing
- 3D hybrid nanoarchitectures
- 2D/3D/hybrid nanodevice integration and manufacturing, with defect and fault tolerance
- Nanodevice and nano-circuit models, methodologies and computer aided design (CAD) tools
- Nanodevice for biomedical applications
- Integration of nanosensors with nanoelectronics
- Fundamental limits of computing at the nanoscale

*** Important Dates ***

- Paper submission: **April 10, 2013**
- Acceptance notification: May 17, 2013
- Early registration deadline: June 8, 2013
- Final version: June 8, 2013

Authors are invited to submit papers of up to 6 pages in length for the Regular Paper Sessions and 2 pages in length for the Concept Paper Sessions in PDF version, double column, IEEE format, with a minimum font size of 10 points on the symposium submission website. Author may choose to make submissions anonymous, although that is not mandatory. The electronic submission will be considered evidence that upon acceptance, the author(s) will present their paper at the symposium. Accepted papers will be included in the Symposium Proceedings, published in *IEEE Xplore* and will be considered for the *NANOARCH Best Paper Awards*. Extended versions of the most exciting papers will be published (subject to a further review process) in a NANOARCH 2013 special section in IEEE Transactions on Emerging Topics in Computing (TETC).

GENERAL CHAIR: Ramesh Karri, Polytechnic Institute of New York University, USA
Csaba Andras Moritz, UMass in Amherst, USA
PROGRAM CHAIR: Swarup Bhunia, Case Western Reserve University, USA
Kaushik Roy, Purdue University, USA