Call for Papers

NANOARCH 2015

11th ACM/IEEE International Symposium on Nanoscale Architectures

July 8-10, 2015, Boston, USA

http://nanoarch.org

NANOARCH is the annual cross-disciplinary forum for the discussion of novel post-CMOS and advanced nanoscale CMOS directions. The symposium seeks papers on innovative ideas for solutions to the principal challenge facing integrated electronics in the 21st century – how to design, fabricate, and integrate nanosystems to overcome the fundamental limitations of CMOS. In particular, such systems could (1) contain unconventional nanodevices with unique capabilities, including directions beyond simple switches, (2) introduce new logic and memory concepts, (3) involve novel circuit styles, (4) introduce new concepts for computing, (5) explore security architectures with nanotechnology, (6) reconfigure and/or mask faults at much higher rates than in CMOS, (7) involve new paradigms for manufacturing, and (8) rethink the methodologies and design tools involved.

This 11th symposium will incorporate several exciting special sessions (e.g., beyond charge-based computing, benefits and challenges with emerging memory devices, and nanoelectronics for biomedical systems) and opportunities for interaction. In addition to Regular Papers (of up to 6 pages in length), we also invite 2-page Concept Papers in the area of nanofabrication, nano-computing, and emerging applications of nanosystems for presentation in Special Sessions. These concept papers would present less-developed but radical and highly innovative work.

Example **topics** (both theoretical and experimental) of interest include (but are not limited to):

- Novel nanodevices and manufacturing/integration ideas with a focus on nanoarchitectures
- Nanoelectronic circuits, nanofabrics, computing paradigms and nanoarchitectures
- Paradigms and nanoarchitectures for computing with unpredictable devices
- Security architectures with nanofabrics
- Reliability aware computing
- 3D hybrid nanoarchitectures
- 2D/3D/hybrid nanodevice integration and manufacturing, with defect and fault tolerance
- Nanodevice and nanocircuit models, methodologies and computer aided design tools
- Fundamental limits of computing at the nanoscale

Important Dates

- **Paper submission: April 10, 2015**
- **Acceptance notification: May 10, 2015**
- **Early registration deadline: June 1, 2015**
- **Final version: June 1, 2015**

Authors are invited to submit papers of up to 6 pages in length for the Regular Paper Sessions and 2 pages in length for the Concept Paper Sessions in PDF version, double column, IEEE format, with a minimum font size of 10 points on the symposium submission website. Author may choose to make submissions anonymous, although that is not mandatory. The electronic submission will be considered evidence that upon acceptance, the author(s) will present their paper at the symposium. Accepted papers will be considered for the NANOARCH Best Paper Awards. Conference content will be submitted for inclusion into IEEE Xplore as well as other Abstracting and Indexing (A&I) databases.

GENERAL CHAIR: Csaba Andras Moritz, *UMass in Amherst, USA*

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